

LS40 ICL Schematics

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,.....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

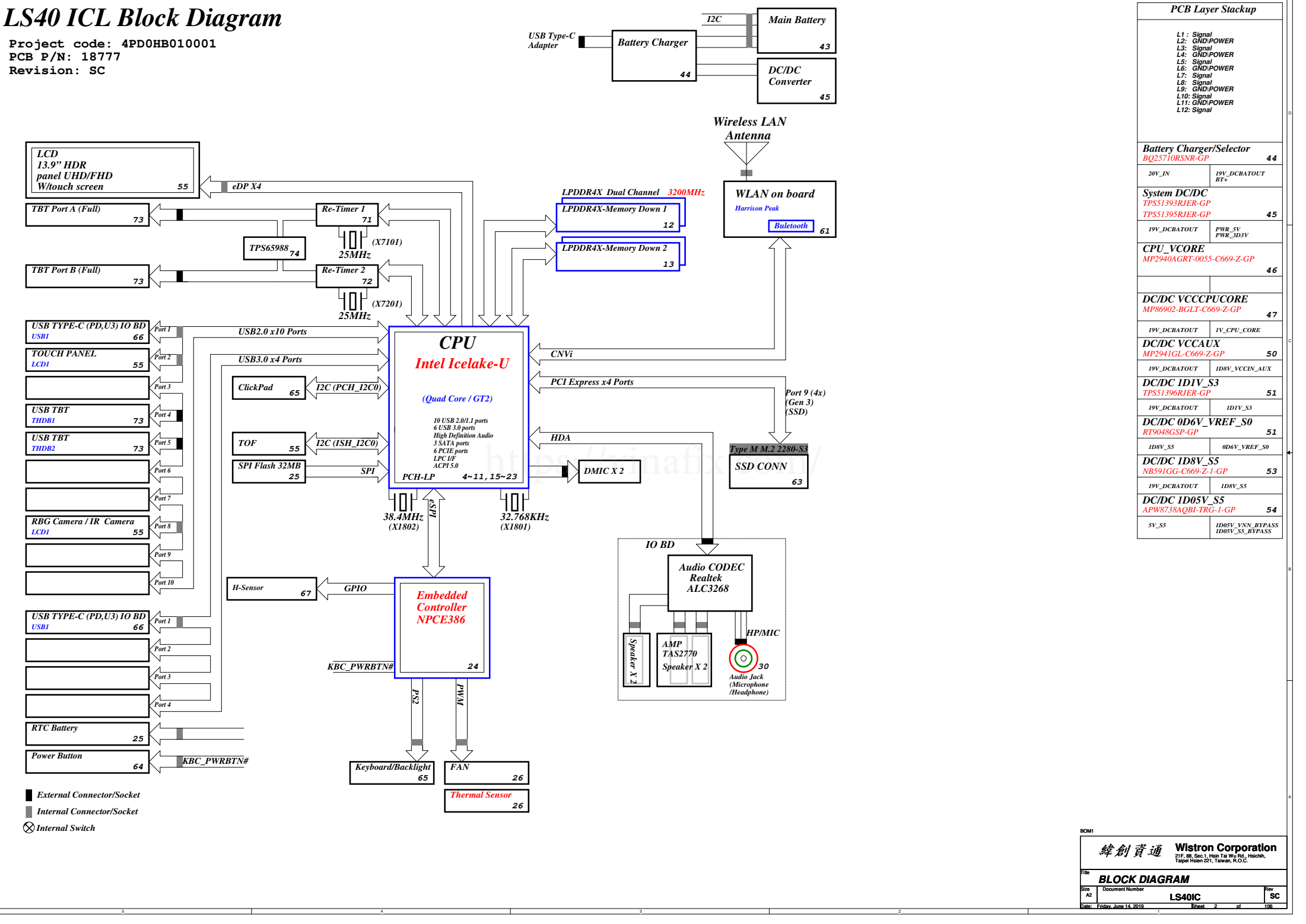
DY	DUMMY
386	NPCE386
388	NPCE388
PSL	Power Switched Logic
Non-PSL	Non Power Switched Logic
BYPASS	Internal Voltage Regulator
Non-BYPASS	External Voltage Regulator
BC1.2	USB Battery Charging 1.2
Non-BC1.2	Non USB Battery Charging 1.2
WLAN-PS	Power Saving Mode
WLAN-NonPS	Non Power Saving Mode
MEM_ID	Memory ID (BOM Control)
Model_ID	Model ID (BOM Control)
PCB_VERSION	PCB VERSION (BOM Control)
FIP	Flexible Instrumented Platform - For power consumption test

BOM1

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Title COVER PAGE			
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LS40 ICL Block Diagram

Project code: 4PD0HB010001
PCB P/N: 18777
Revision: SC



PCB Layer Stackup	
L1 : Signal	
L2: GND/POWER	
L3: Signal	
L4: GND/POWER	
L5: Signal	
L6: GND/POWER	
L7: Signal	
L8: Signal	
L9: GND/POWER	
L10: Signal	
L11: GND/POWER	
L12: Signal	

Battery Charger/Selector	
BQ25710RSNR-GP 44	
20V_IN	19V_DCBATOUT BT+

System DC/DC	
TPS51393R1ER-GP 45	
TPS51395R1ER-GP	
19V_DCBATOUT	PWR_5V PWR_3D3V

CPU_VCORE	
MP2940AGRT-0055-C669-Z-GP 46	

DC/DC VCCCPUCORE	
MP86902-BGLT-C669-Z-GP 47	
19V_DCBATOUT	1V_CPU_CORE

DC/DC VCCAUX	
MP2941GL-C669-Z-GP 50	
19V_DCBATOUT	ID8V_VCCIN_AUX

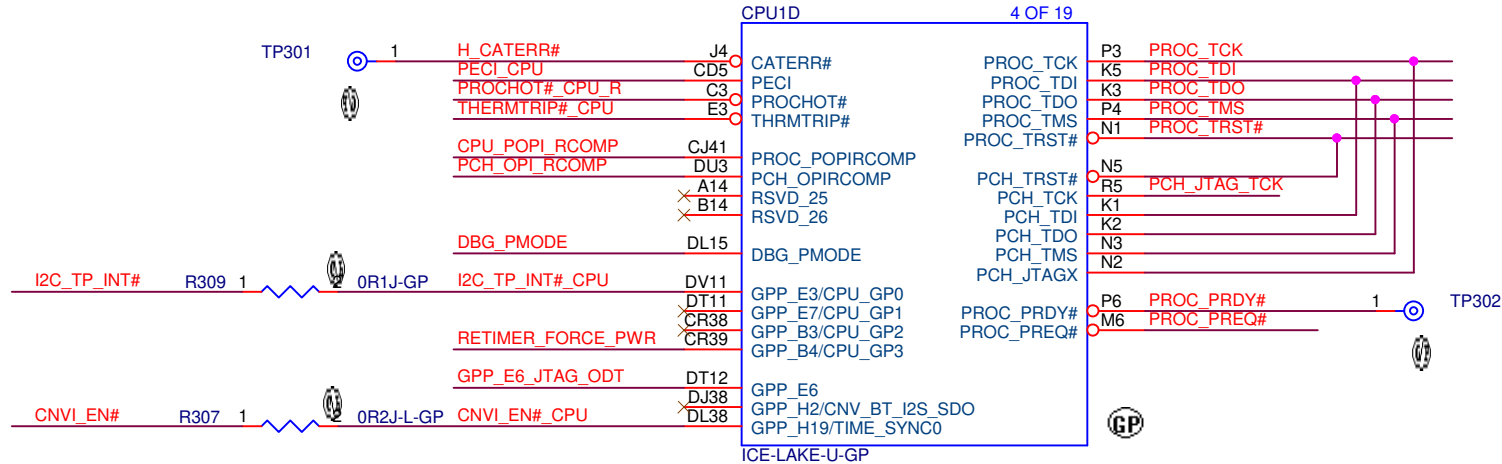
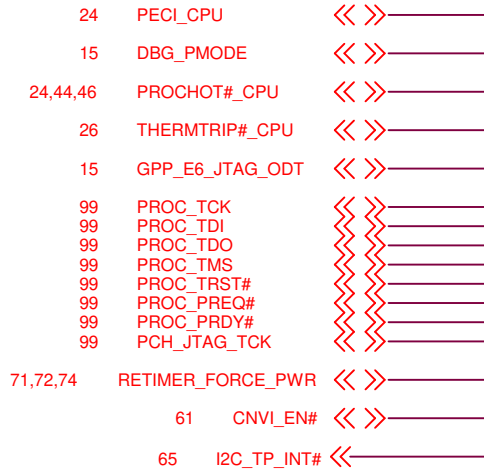
DC/DC ID1V_S3	
TPS51396R1ER-GP 51	
19V_DCBATOUT	ID1V_S3

DC/DC 0D6V_VREF_S0	
RT9048GSP-GP 51	
ID8V_S5	0D6V_VREF_S0

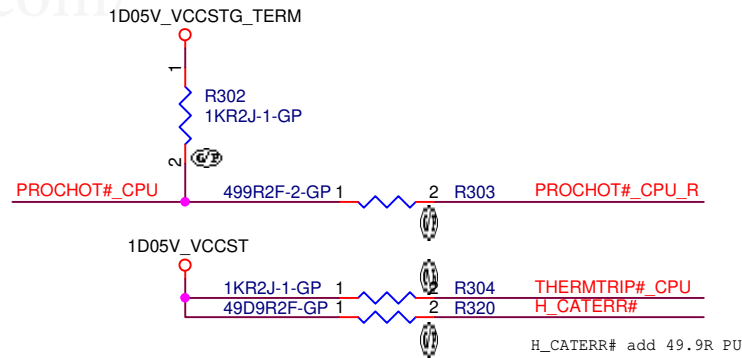
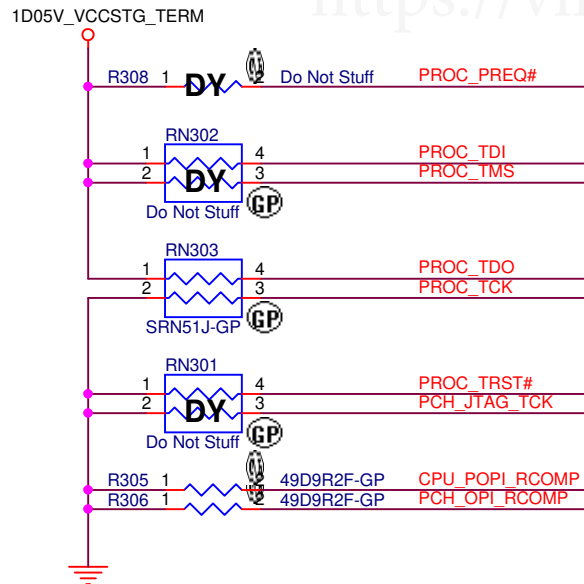
DC/DC ID8V_S5	
NB591GG-C669-Z-1-GP 53	
19V_DCBATOUT	ID8V_S5

DC/DC ID05V_S5	
APW8738AQBI-TRG-1-GP 54	
5V_S5	ID05V_VNN_BYPASS ID05V_S5_BYPASS

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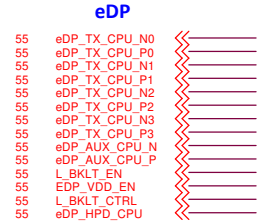
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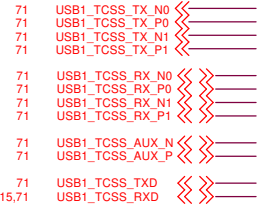
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Title CPU (THML/JTAG)			
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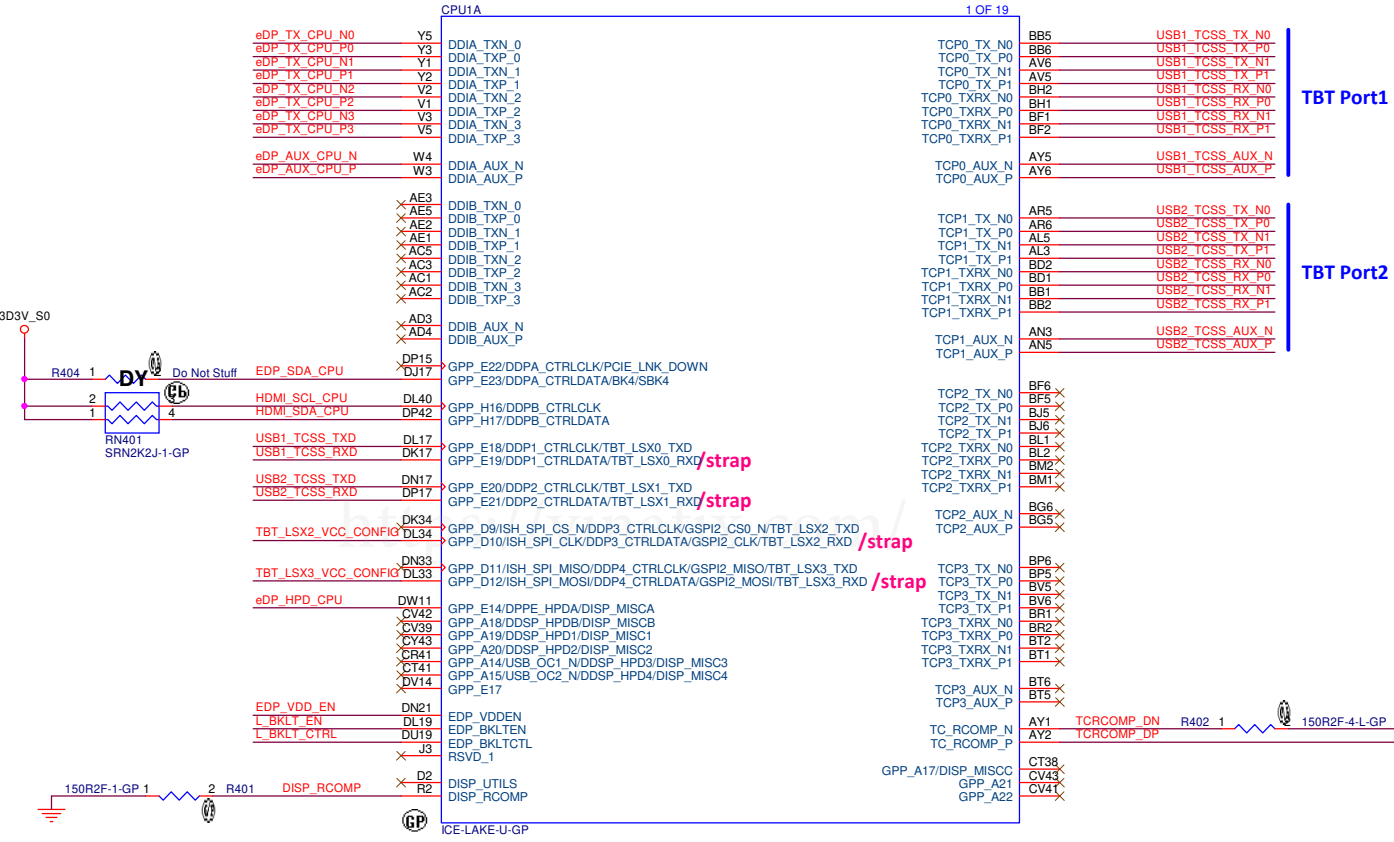
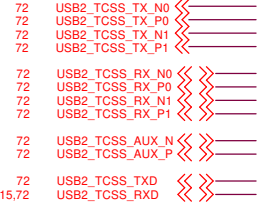
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TBT Port1 (TBT/USB3.1/DP/PD)



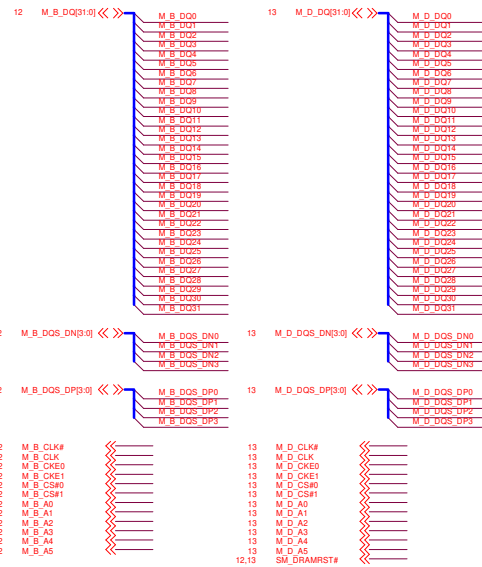
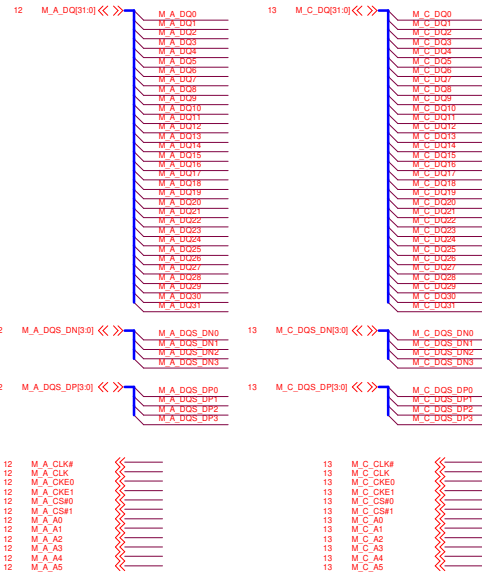
TBT Port2 (TBT/USB3.1/DP/PD)



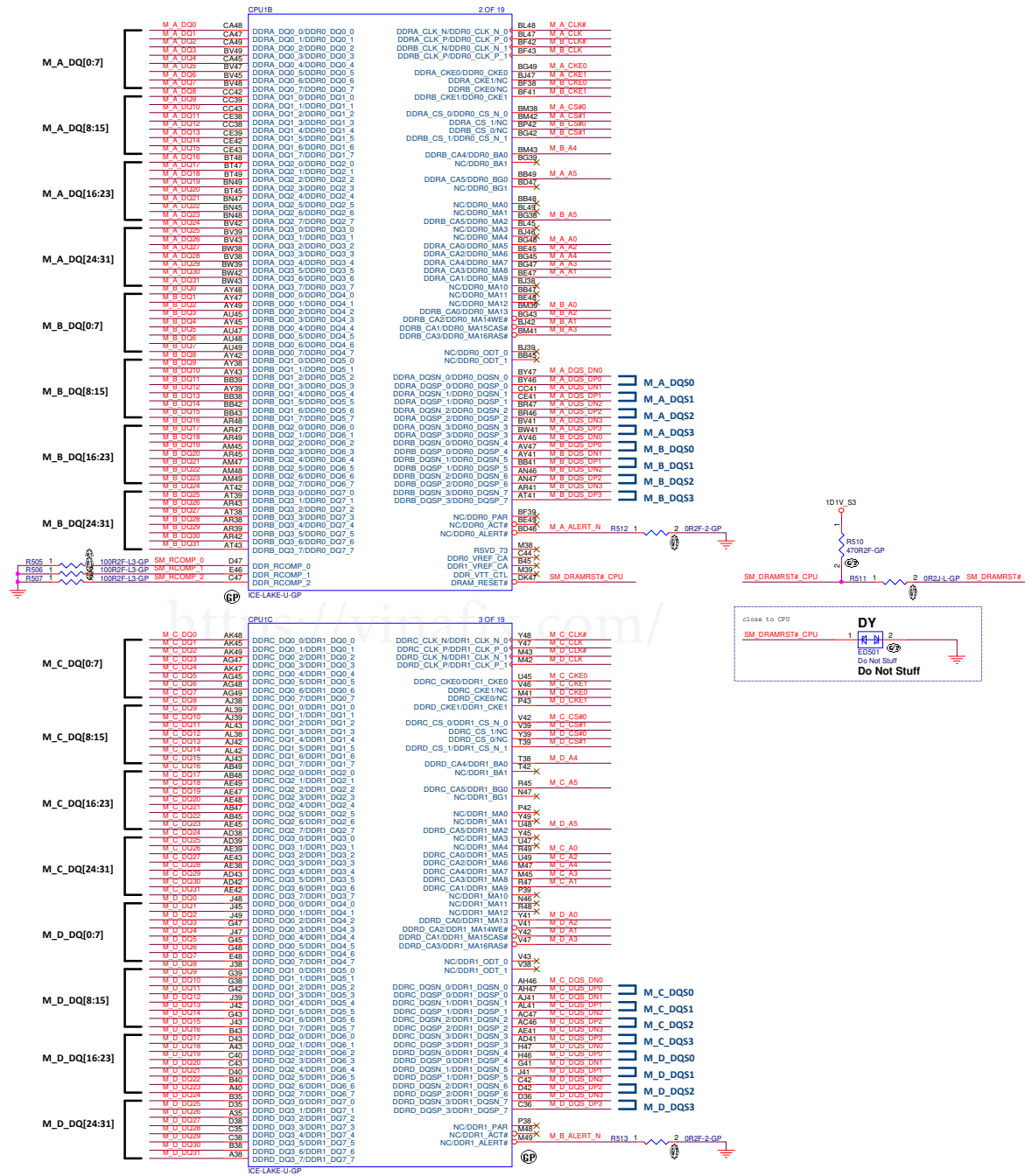
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LPDDR4x ball type: Non-Interleaved

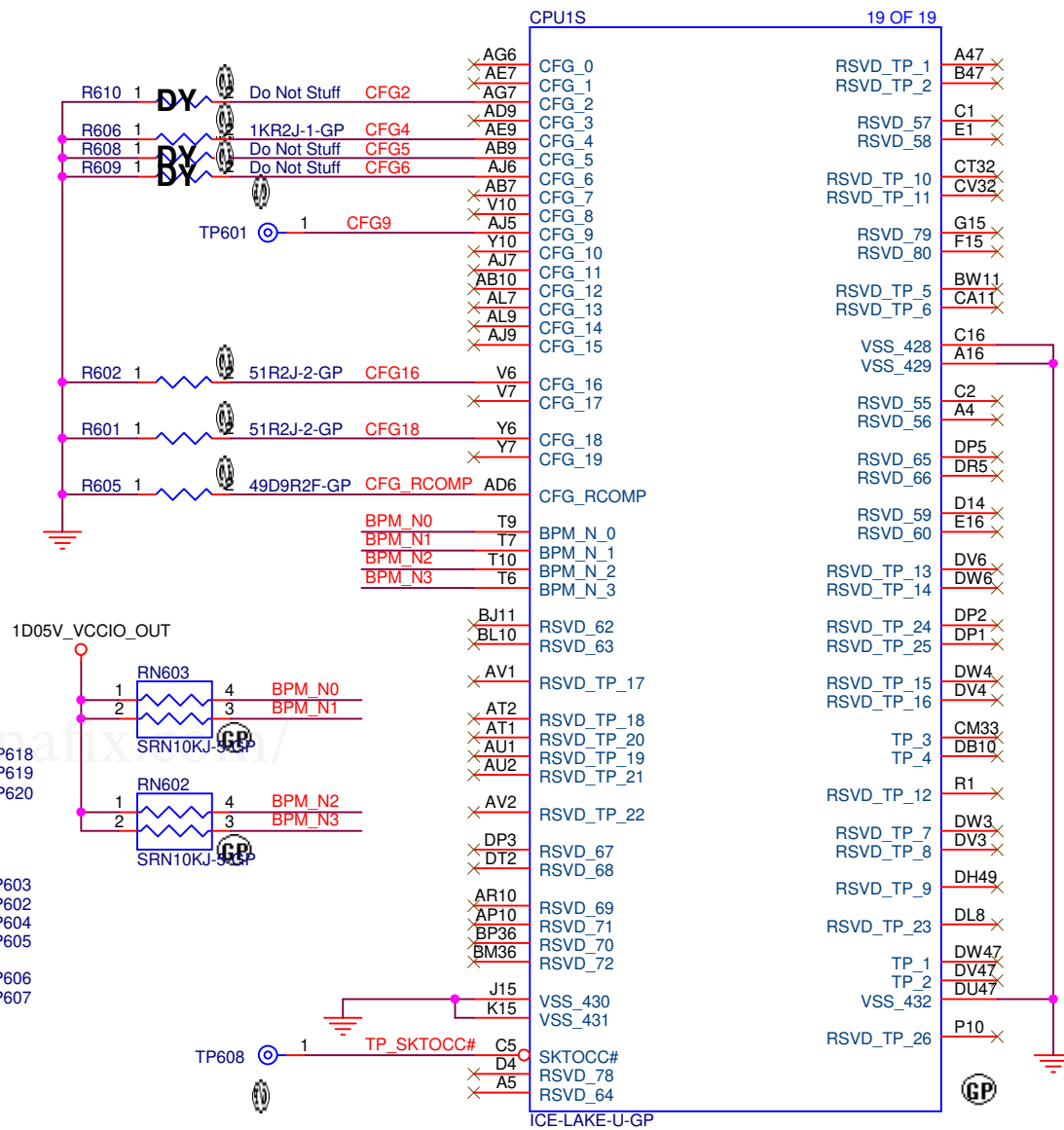


BOM1

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT)NORMAL OPERATION;
	0: LANE REVERSAL

DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED
	AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1: DISABLED
	NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
	10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
	01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED



BOM1

Title	CPU (CFG/IST)
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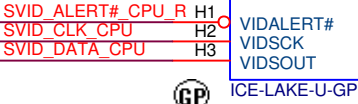
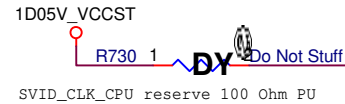
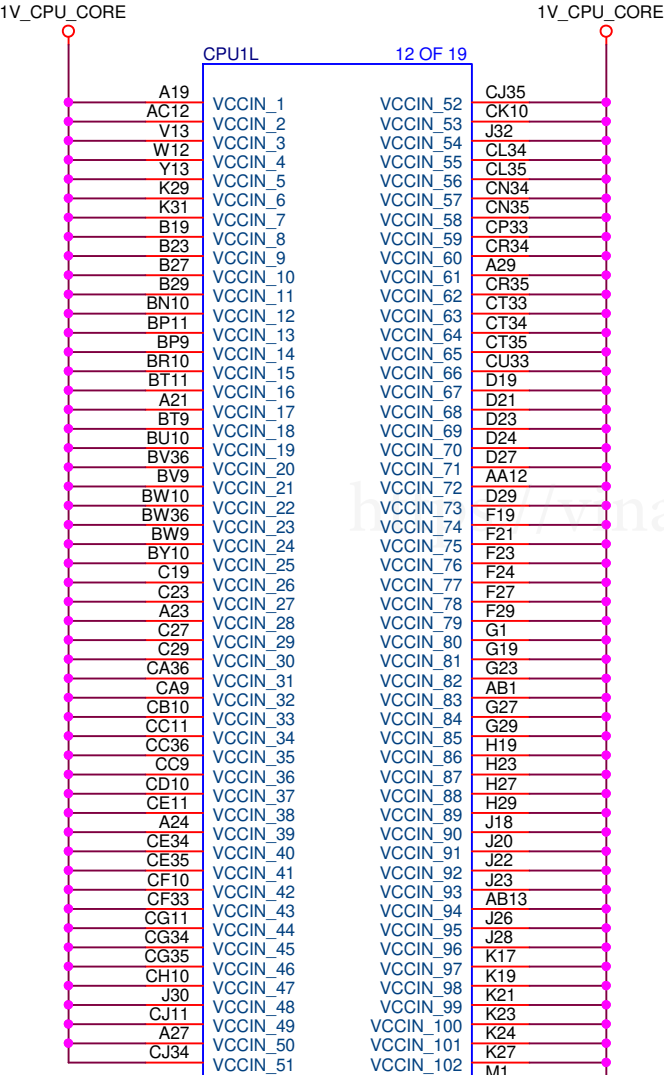
Size	Document Number	Rev
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A4	LS40IC	SC
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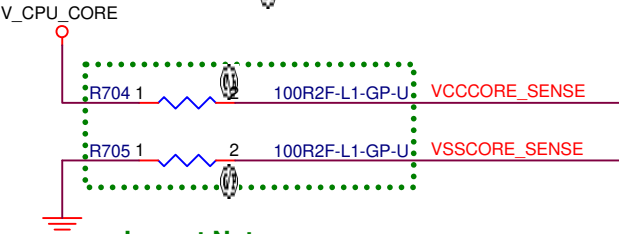
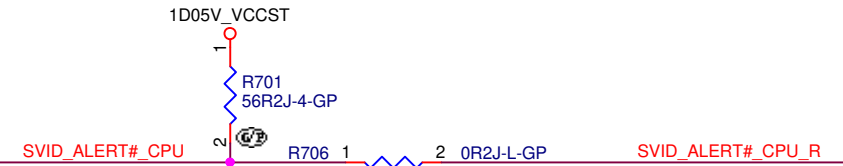
46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_CLK_CPU
46 SVID_DATA_CPU
46 SVID_ALERT#_CPU



SVID DATA



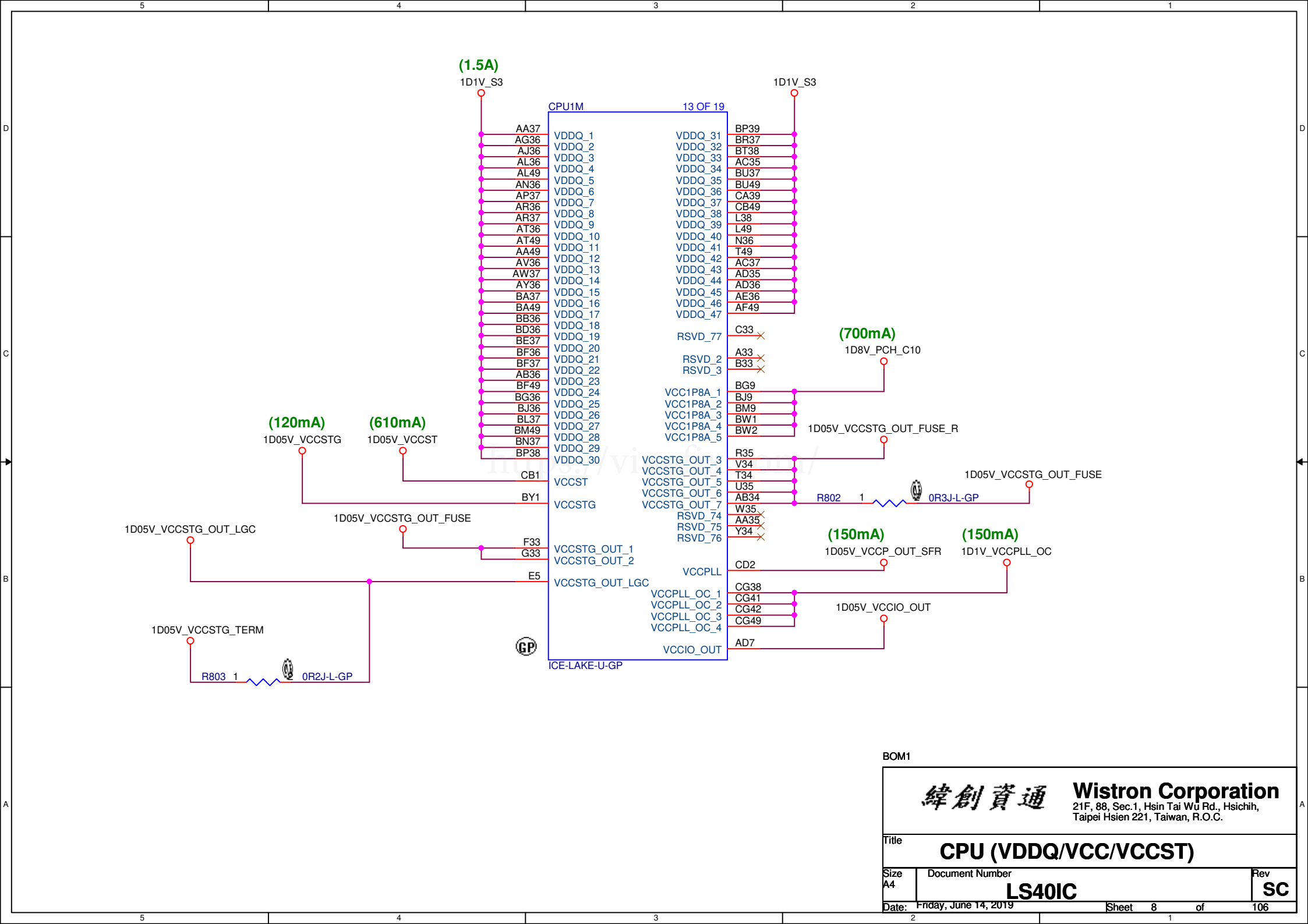
SVID ALERT



Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

BOM1

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Title			
CPU (VCCIN/VID)			
Size A4	Document Number LS40IC		Rev SC
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Title			
CPU (VDDQ/VCC/VCCST)			
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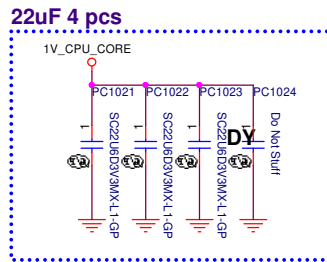
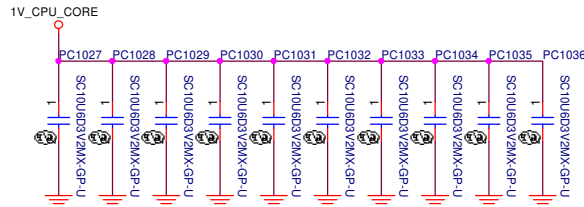
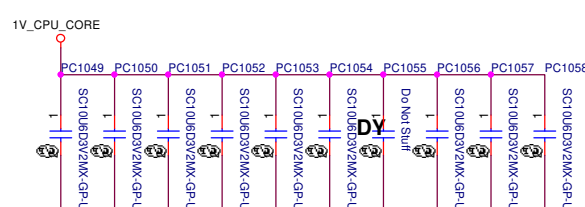
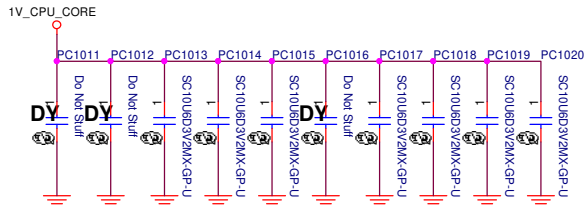
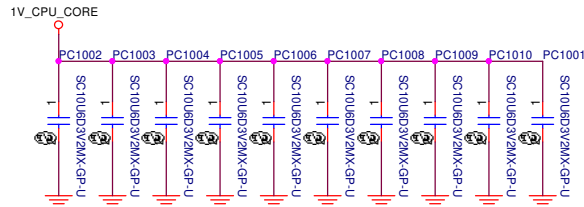
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Title <div>CPU (RSVD)</div>	
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Main Func = CPU

U42
IccMax current-10ms max = 62A

U42	PCS	Cap
22uF	4	330uF*2
10uF	40	

VCORE

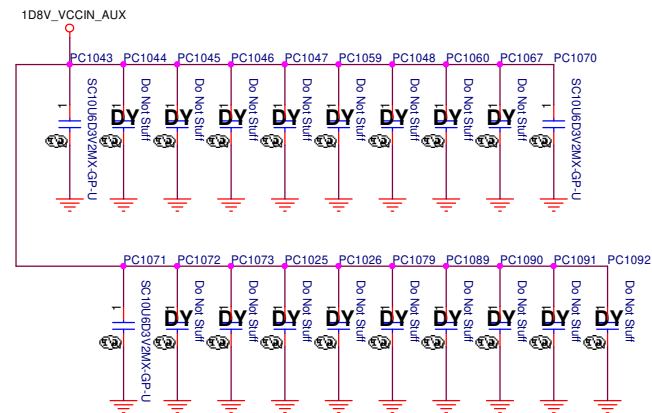
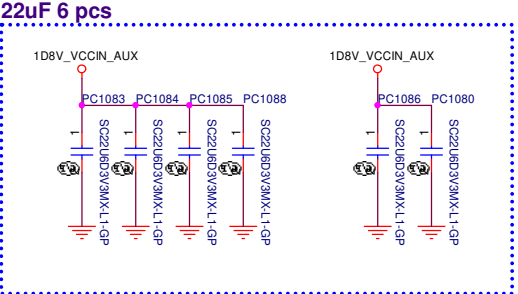
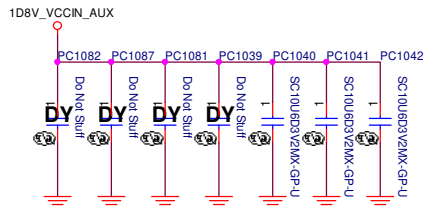
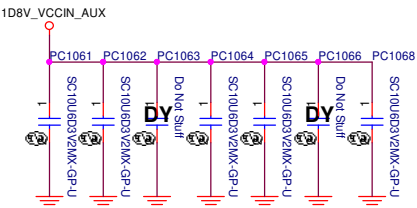
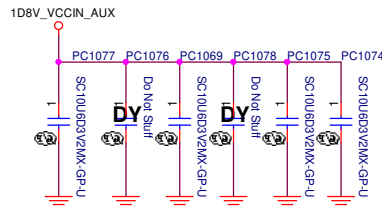


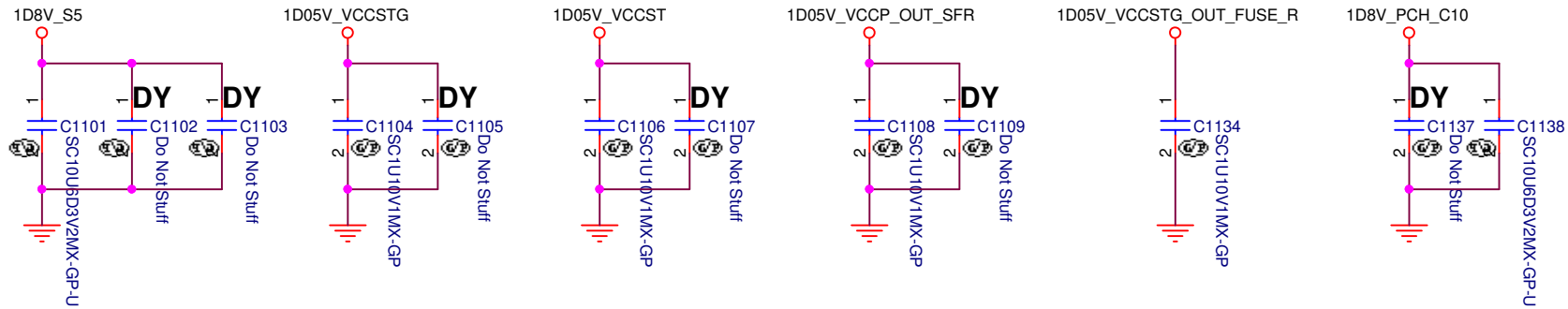
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1D8V_VCCIN_AUX

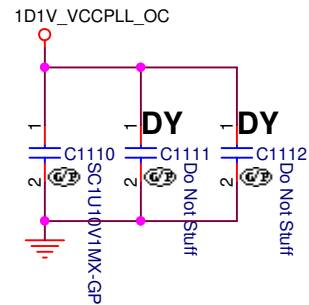
U42
IccMax current-10ms max = 31A

U42	PCS	Cap
22uF	6	220uF*1
10uF	40	

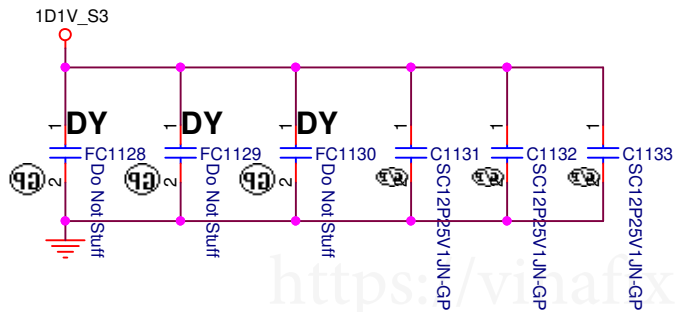




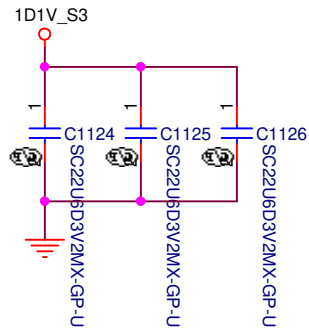
For VCCPLL_OC
pin-CG38,CG41,CG42,CG49



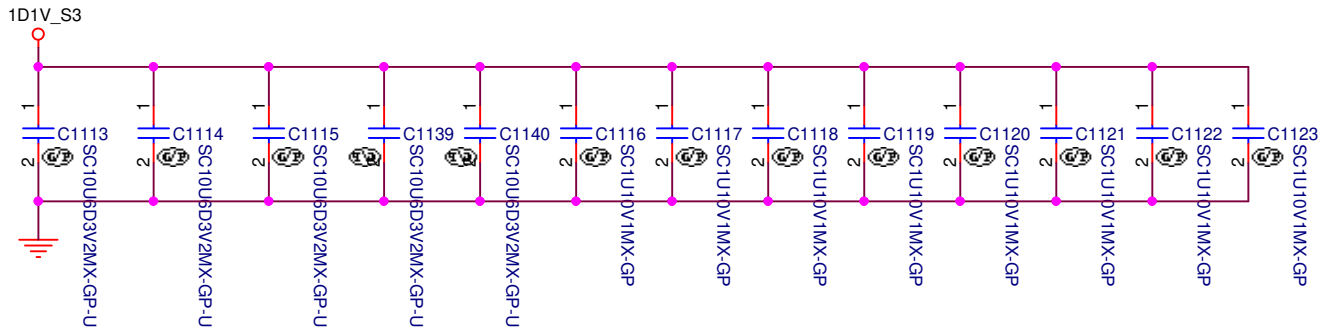
EMC CAPS - PLACE <4mm FROM SOC VDDQ,
WITH EACH PAIR <12mm APART



PLACE on CPU Same Side



PLACE on BACK SIDE



BOM1

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Title CPU (Power CAP2)		
Size A4	Document Number LS40IC	Rev SC
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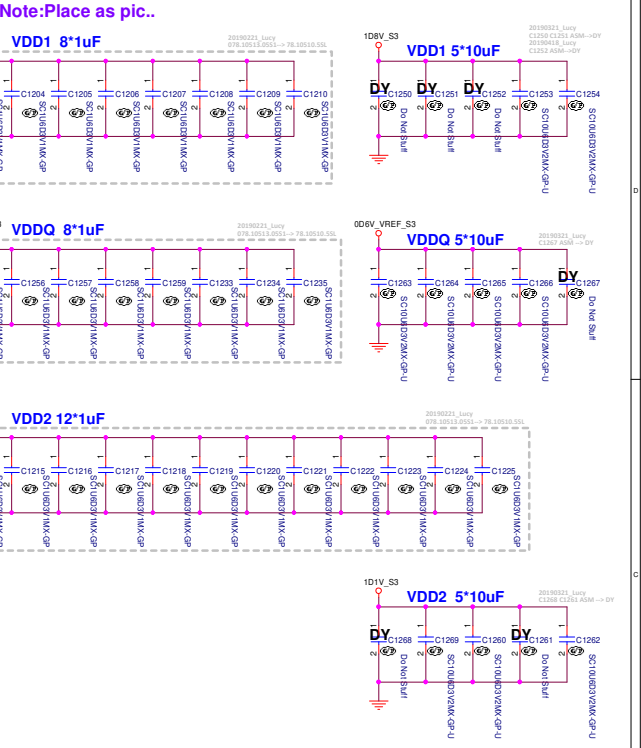
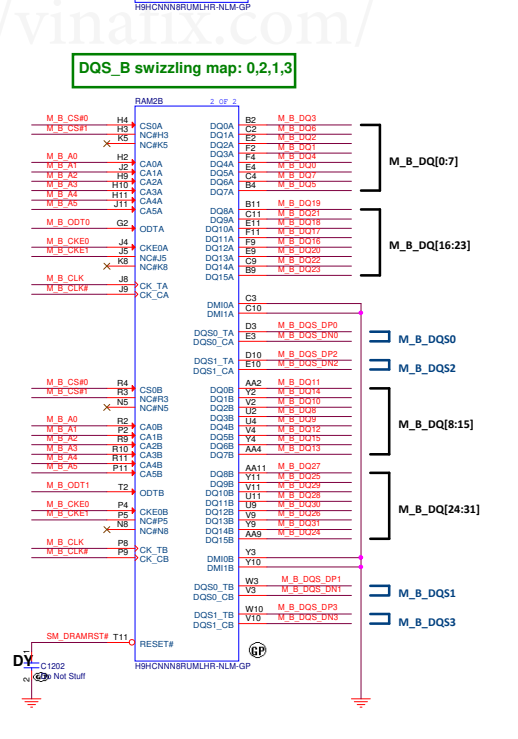
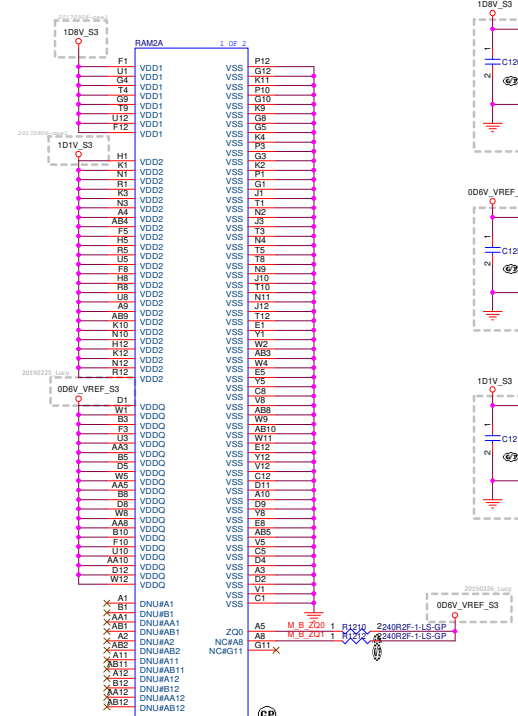
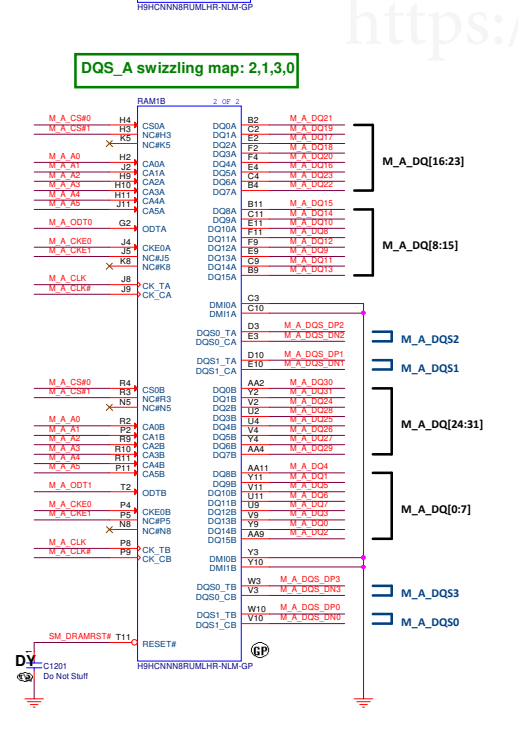
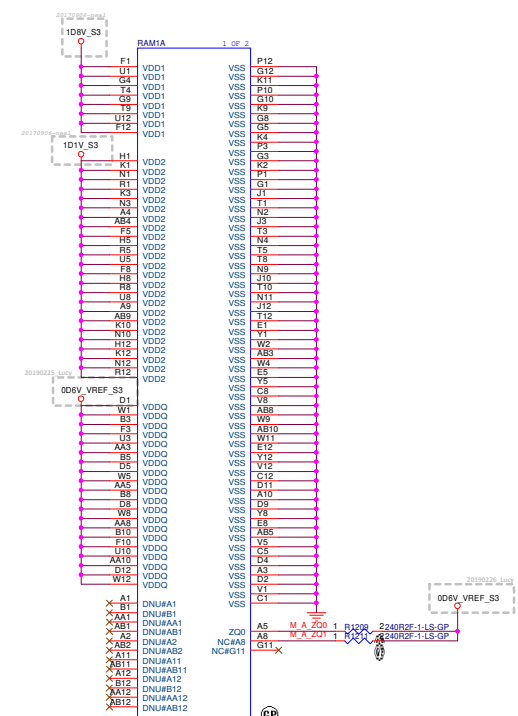
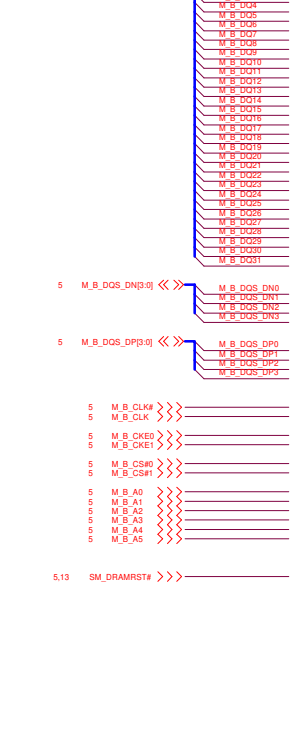
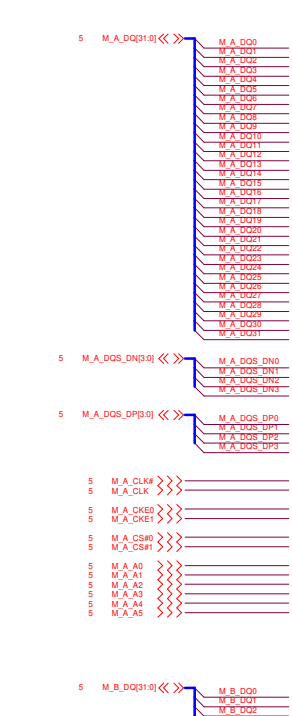
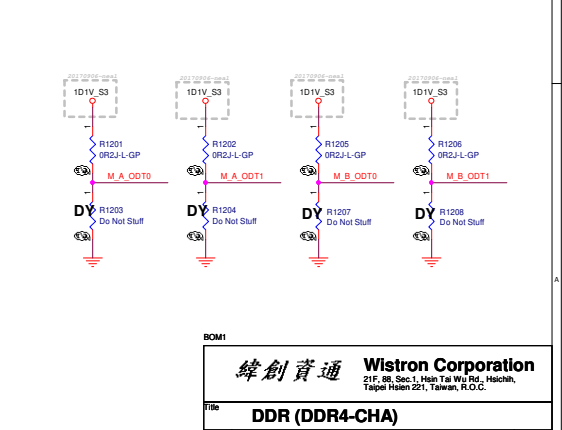


Table 4-28. LPDDR4X Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
LPDDR4X x32	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1 μ F (0402)
		evenly distribute among all Drams	5x 10 μ F (0603)
	VDDQ	4 per Dram, 2 per short edge	16x 1 μ F (0402)
		evenly distribute among all Drams	5x 10 μ F (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1 μ F (0402)
		evenly distribute	5x 10 μ F (0603)

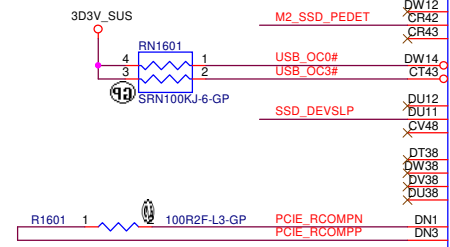
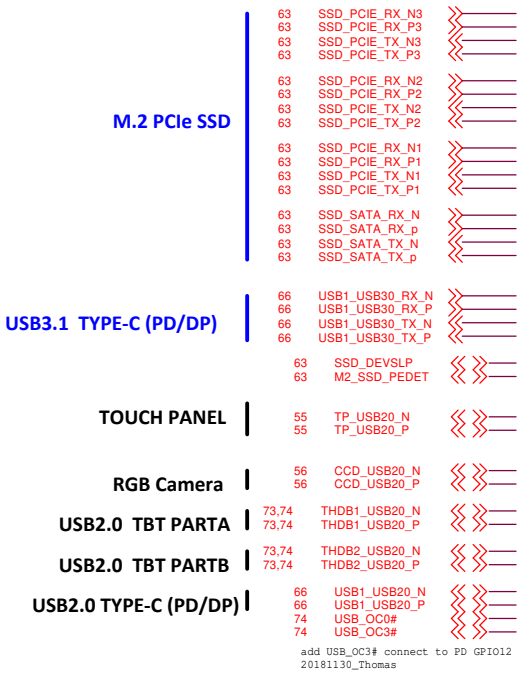


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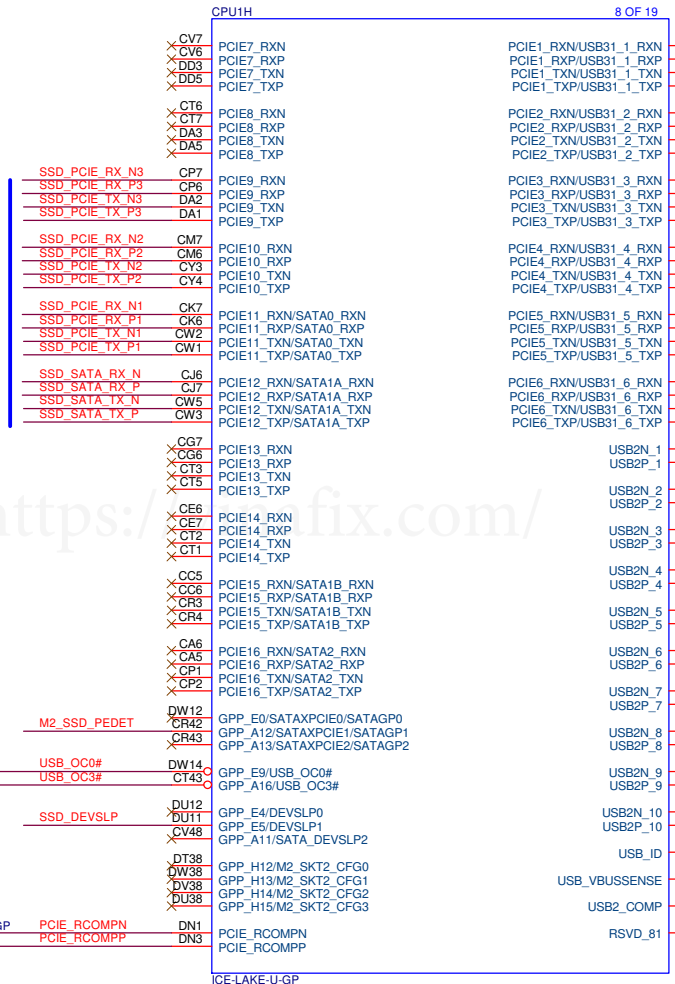
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Title	
DDR (RSVD)	
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M.2 PCIe SSD



For TYPE C, Tony wants to follow S940(WHL) which is connected to USB but has not yet determined that it is still tracking this item. (S940(ICL) may be connected to TCP signal.)

USB3.1 TYPE-C (PD/DP)

USB2.0 TYPE-C (PD/DP)

TOUCH PANEL

USB2.0 TBT PARTA

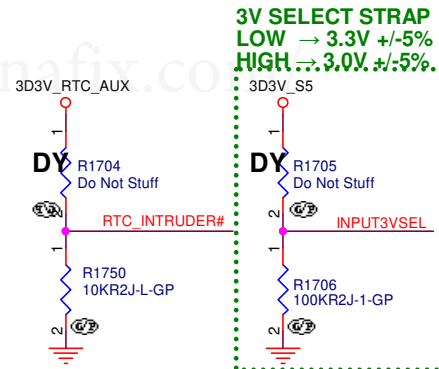
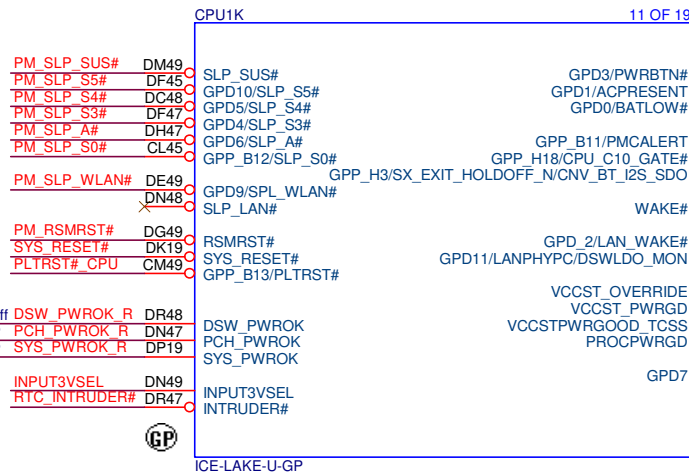
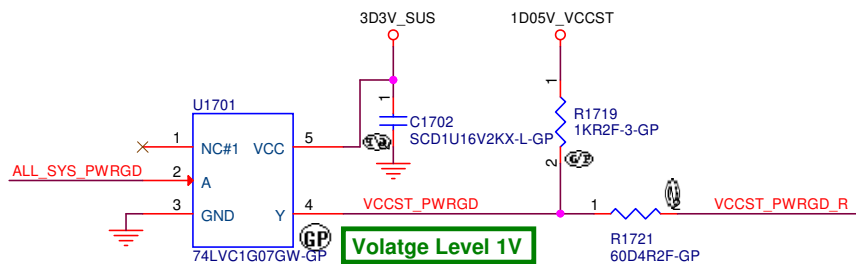
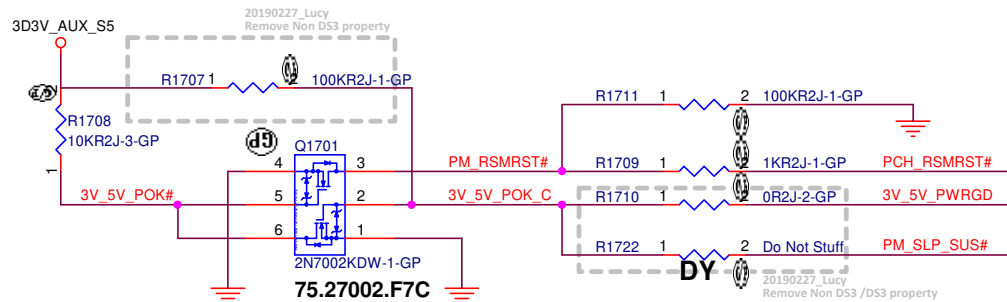
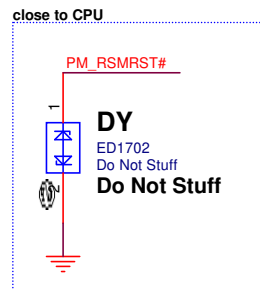
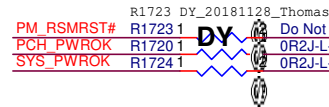
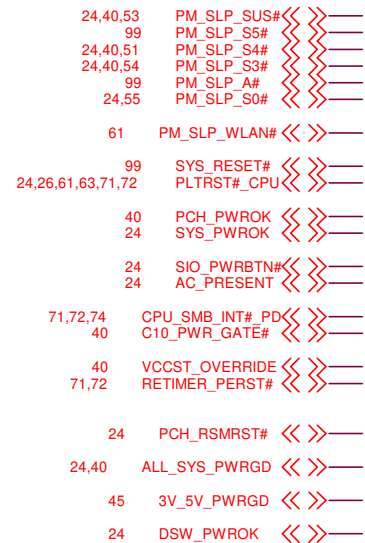
USB2.0 TBT PARTB

RGB Camera

BOM1

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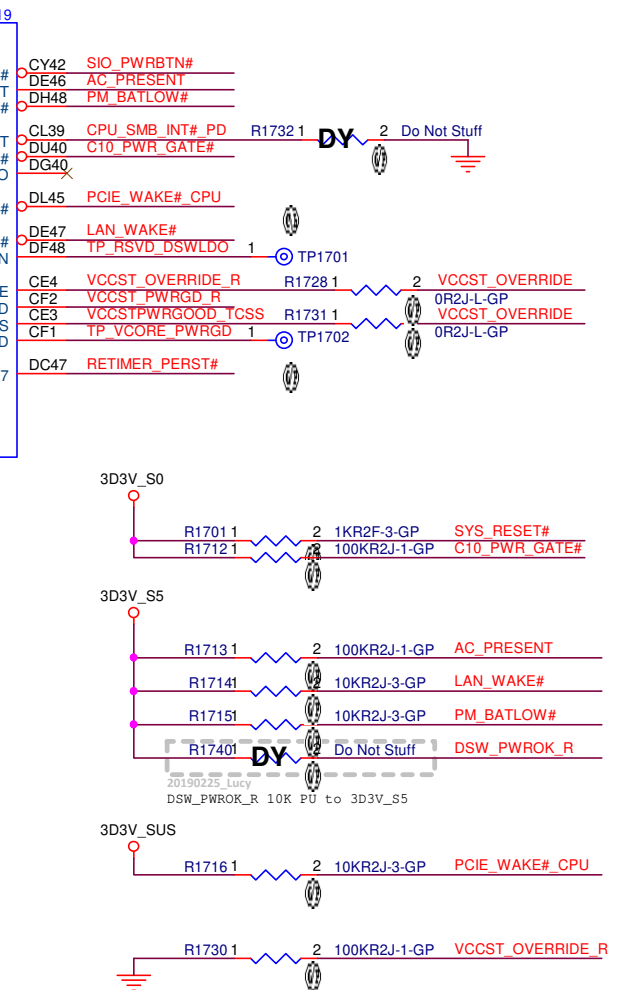
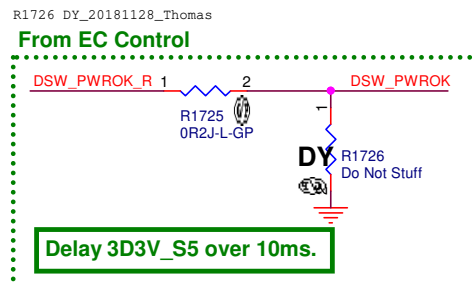


add RTC_INTRUDER# 10K PD_20181129_Thomas

The VCCSPI voltage (3.3V or 1.8V) is selected via a hard strap on the INTRUDER#.

0 = SPI interface operation voltage is 3.3V (ground through a 10 kohm resistor)

1 = SPI interface operation voltage is 1.8V (pulled up with 1 Mohm to VCCRTC)

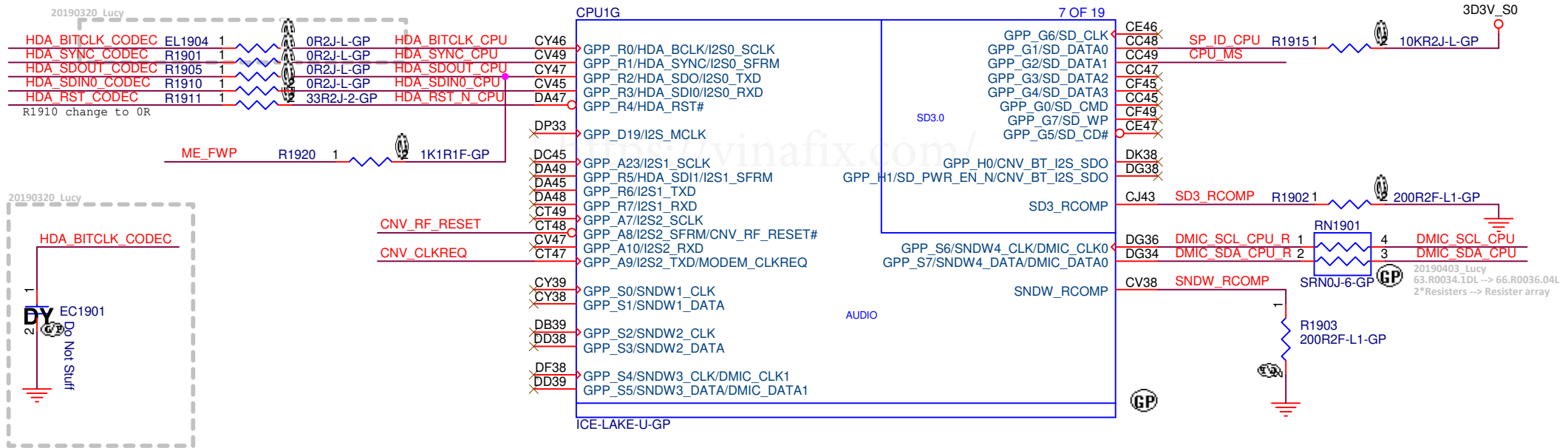
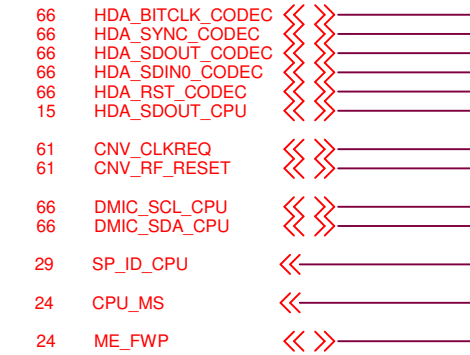


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BOM1

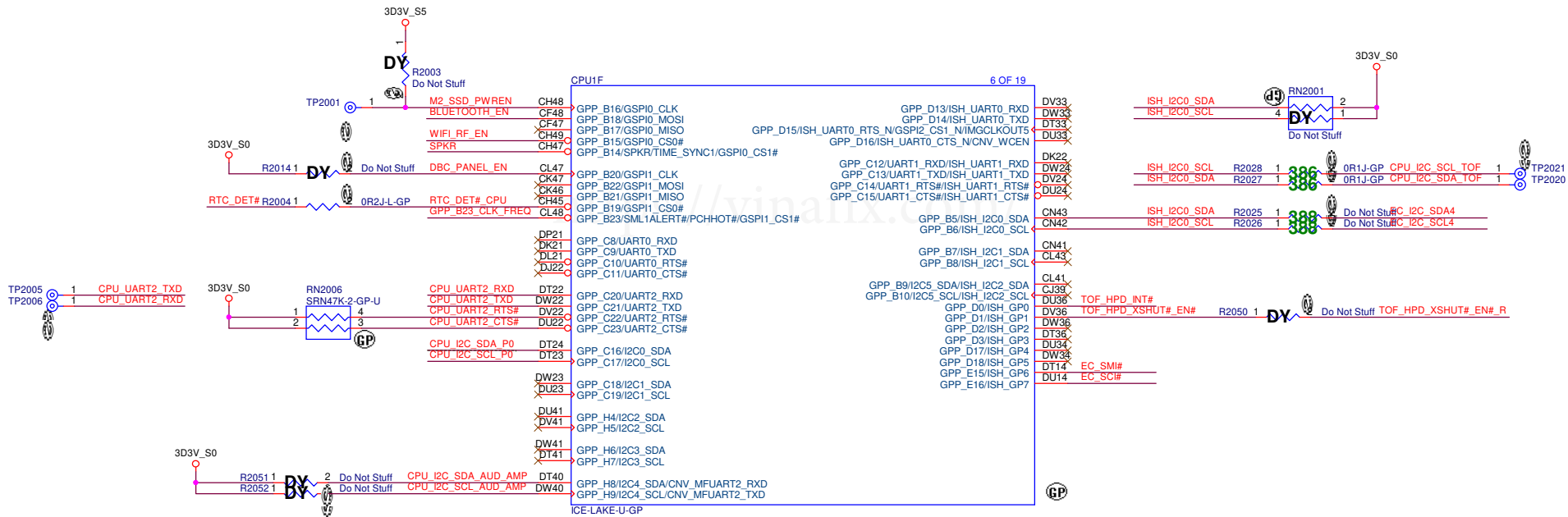
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (HAD/I2S/SD/DMIC)
-------	------------------------------

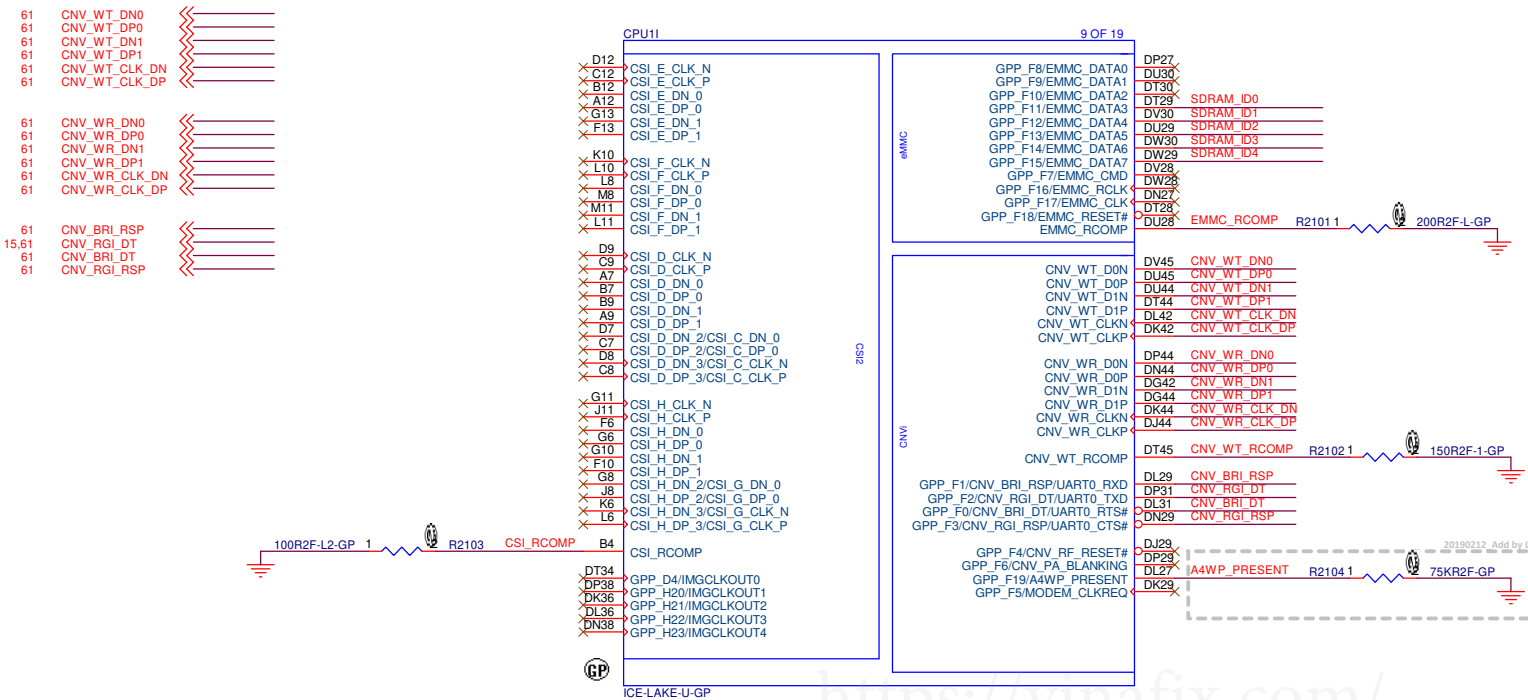
Size A4	Document Number LS40IC	Rev SC
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Date: Friday, June 14, 2019 Sheet 19 of 106

15	GPP_B23_CLK_FREQ	<< >>	
25	RTC_DET#	<< >>	
24,66	SPKR	<< >>	
61	BLUETOOTH_EN	<< >>	
24,61	WIFI_RF_EN	<< >>	
24,67	LID_CLOSE#	<< >>	
24,46	EC_I2C_SDA4	<< >>	
24,46	EC_I2C_SCL4	<< >>	
24,55	CPU_I2C_SDA_TOF	<< >>	
24,55	CPU_I2C_SCL_TOF	<< >>	
55	TOF_HPDP_XSHUT#_EN#_R	<< >>	
55	TOF_HPDP_INT#	<< >>	
65	CPU_I2C_SDA_P0	<< >>	
65	CPU_I2C_SCL_P0	<< >>	
66	CPU_I2C_SDA_AUD_AMP	<< >>	
66	CPU_I2C_SCL_AUD_AMP	<< >>	
68	CPU_UART2_TXD	<< >>	
68	CPU_UART2_RXD	<< >>	
24	EC_SMI#	<< >>	
24	EC_SCI#	<< >>	



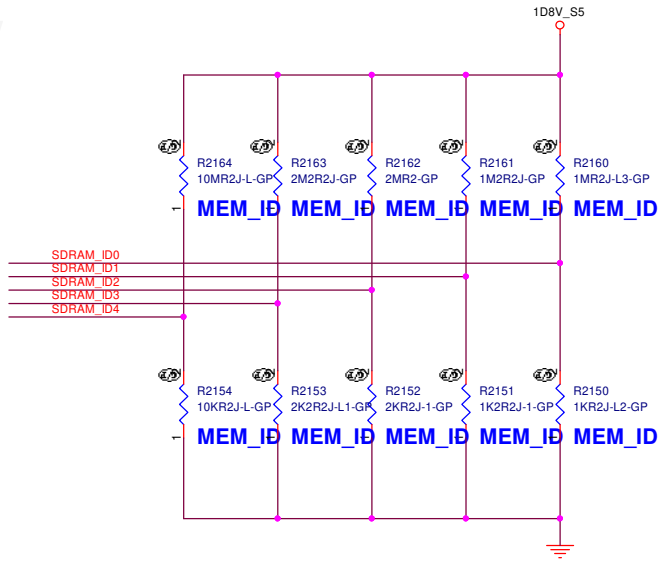
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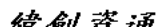


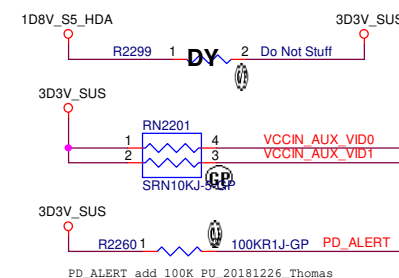
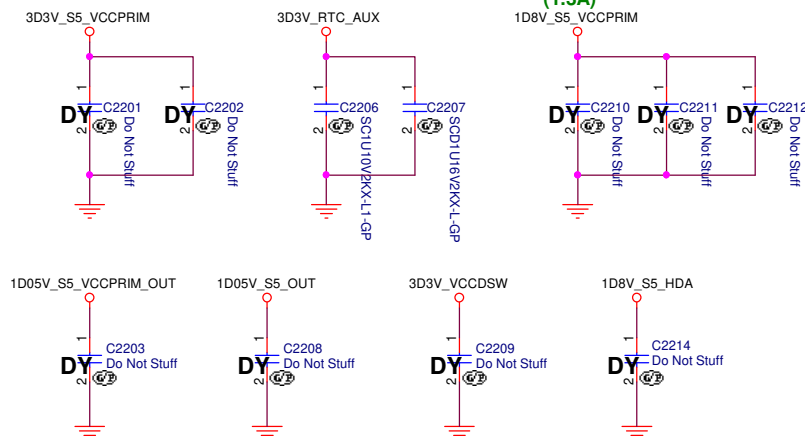
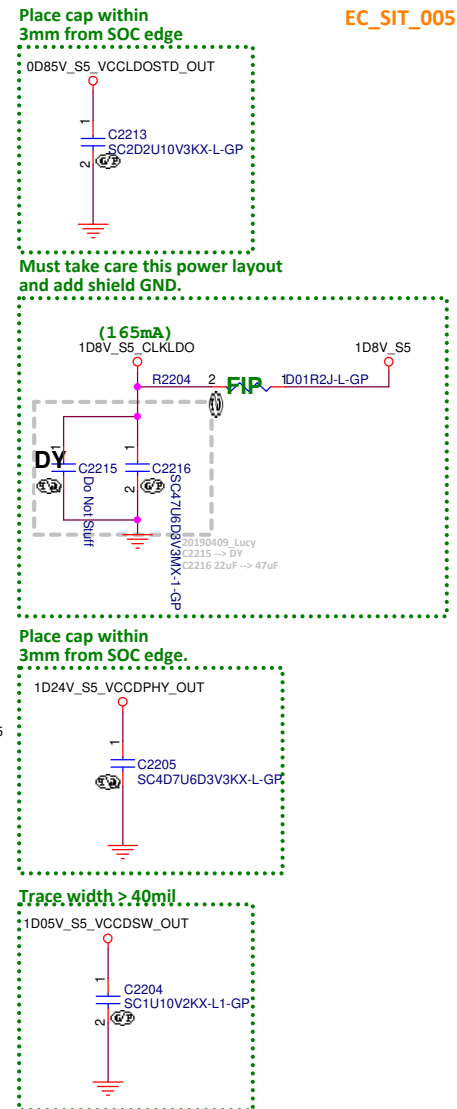
SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Description	Wsrton PN	Vendor	Density
0	0	0	0	0		SM30E51328	Micron	
0	0	0	0	1		SM30N76597	Samsung	
0	0	0	1	0		SM30E51334	SK hynix	
0	0	0	1	1		SM30E51329	Micron	
0	0	1	0	0		SM30N76598	Samsung	
0	0	1	0	1		SM30E51335	SK hynix	

SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Memory ID	Wisrton PN	Vendor	Density
R2164 R2154	R2163 R2153	R2162 R2152	R2161 R2151	R2160 R2150				
10M 10K	2.2M 2.2K	2M 2K	1.2M 1.2K	1M 1K	0	SM30E51328	Micron	
10M 10K	2.2M 2.2K	2M 2K	1.2M 1.2K	1K 1M	1	SM30N76597	Samsung	
10M 10K	2.2M 2.2K	2M 2K	1.2K 1.2M	1M 1K	2	SM30E51334	SK hynix	
10M 10K	2.2M 2.2K	2M 2K	1.2K 1.2M	1K 1M	3	SM30E51329	Micron	
10M 10K	2.2M 2.2K	2K 2M	1.2M 1.2K	1M 1K	4	SM30N76598	Samsung	
10M 10K	2.2M 2.2K	2K 2M	1.2M 1.2K	1K 1M	5	SM30E51335	SK hynix	

Value	Part Number
1K	63.10234.1.0L
1M	63.10534.1.1L
1.2K	63.12234.1DL
1.2M	63.12534.1DL
2K	63.20234.1DL
2M	63.20534.1DL
2.2K	63.22234.1.0L
2.2M	63.22534.1DL
10K	63.10334.1.0L
10M	63.10634.1DL

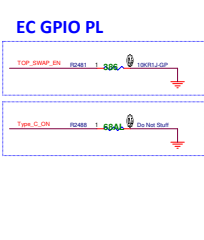
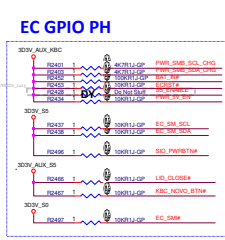
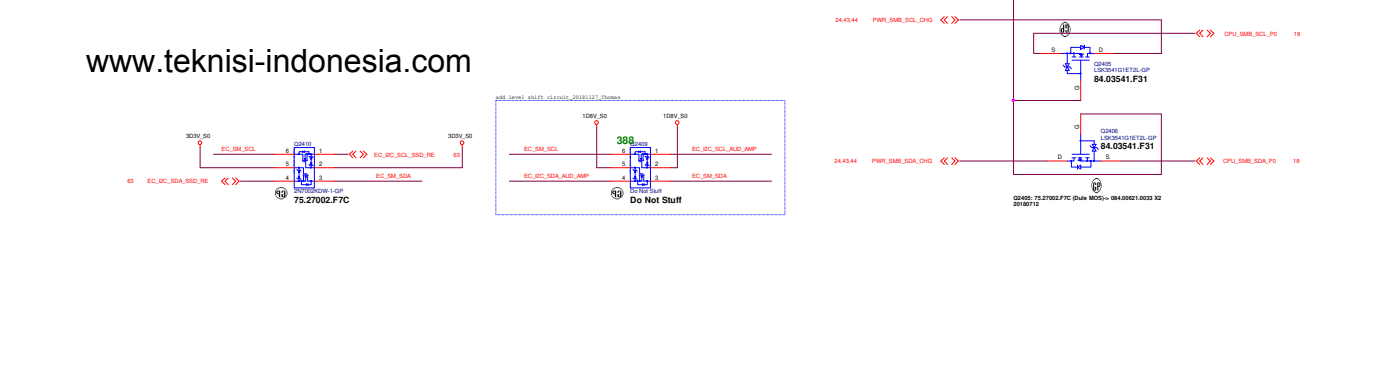
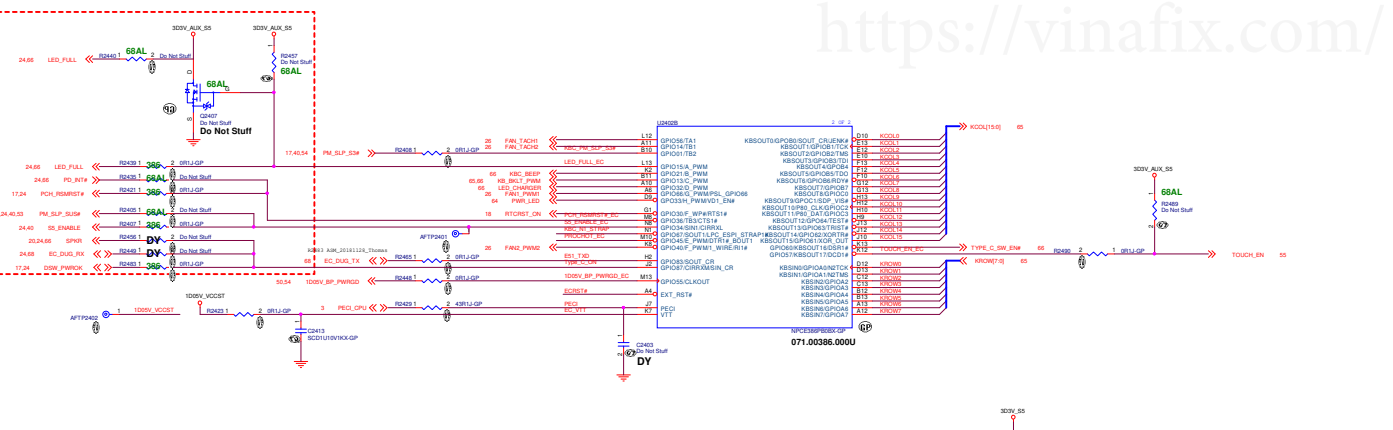
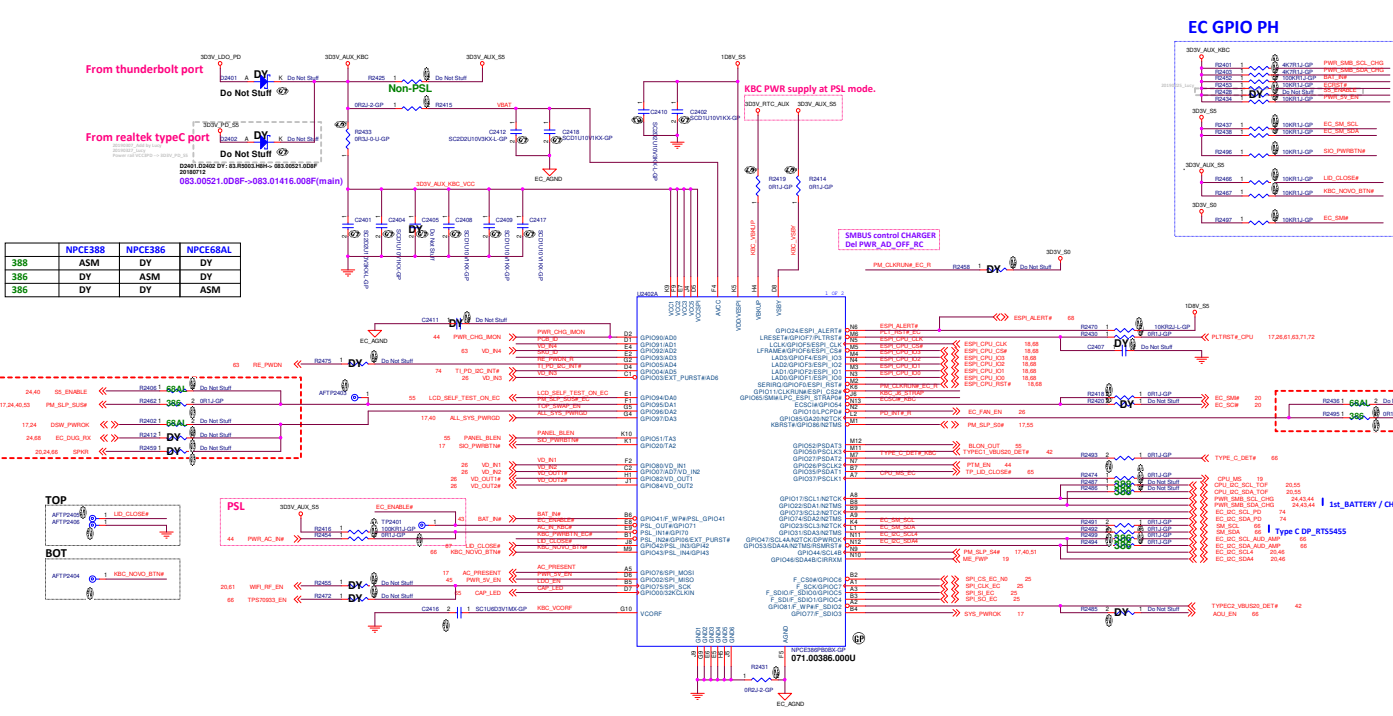


BOM1			
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (CSI/EMMC/CNV1)			
Size A3	Document Number		Rev
	LS40IC		SC
Date:	Friday, June 14, 2019	Sheet	21 of 106



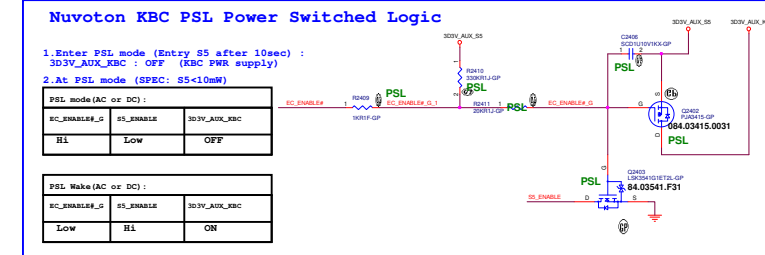
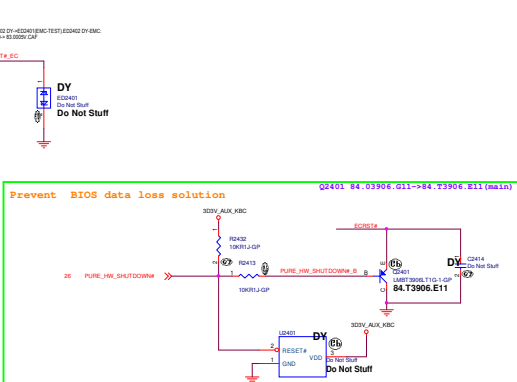


SSID = KBC



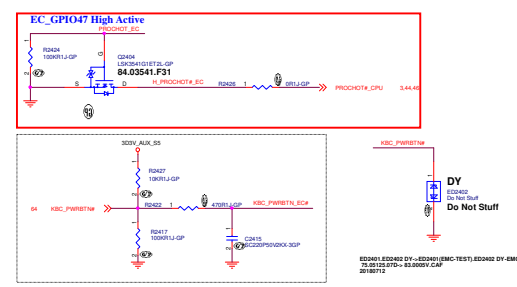
Model_ID_BOM Ctrl			
PCB VERSION (ADP2500)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LSH	100.0K	10.0K	3.0V
NA	100.0K	20.0K	2.75V
NA	100.0K	33.0K	2.48V
NA	100.0K	47.0K	2.24V
NA	100.0K	64.0K	2.0V
NA	100.0K	76.0K	1.87V
NA	100.0K	215.0K	1.65V

PCB VERSION			
PCB VERSION (ADP2500)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
NA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
J	100.0K	64.0K	2.0V
-1M	100.0K	76.0K	1.87V
Reserved	100.0K	100.0K	1.65V



Nuvoton KBC PSL Power Switched Logic			
1. Enter PSL mode (Entry S5 after 10sec):	303V_AUX_KBC	OFF	(KBC PWR supply)
2. At PSL mode (SPEC: S5<10mM)			
PSL mode (AC or DC):			
EC_ENABLE_S	SS_ENABLE	303V_AUX_KBC	
HL	Low	OFF	

PSL Wake (AC or DC):			
EC_ENABLE_S	SS_ENABLE	303V_AUX_KBC	
Low	HL	ON	

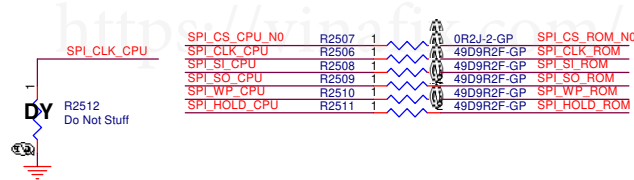
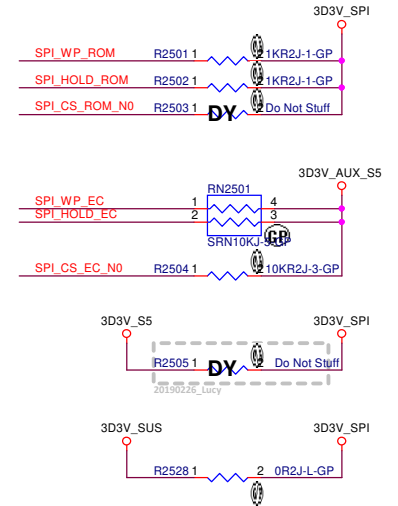
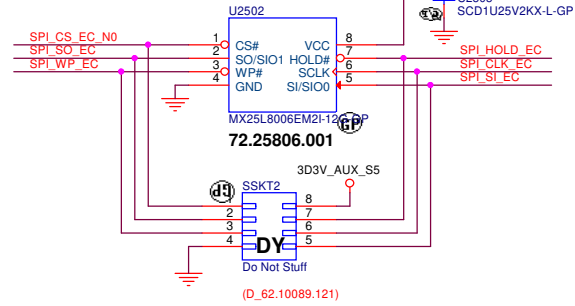
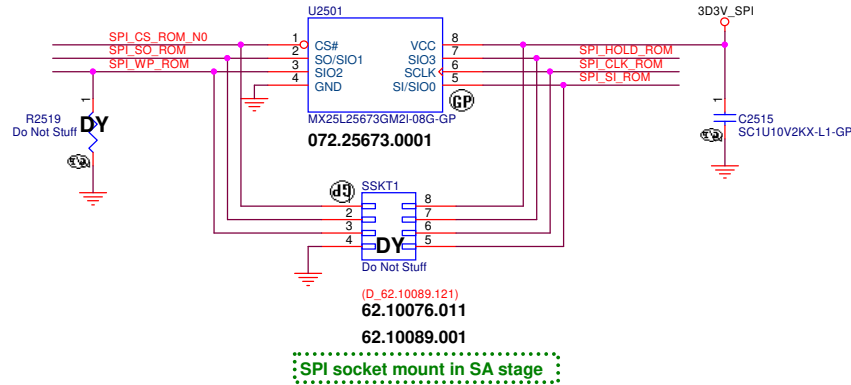
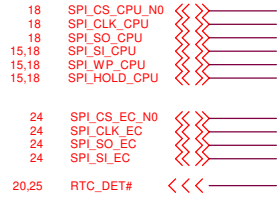


KBC PWRBTN ECH: Low			
(1) 4sec: PWR Button			
shut down (2) 8sec: KBC			
reset			

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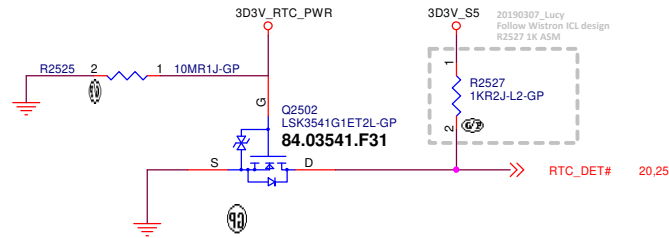
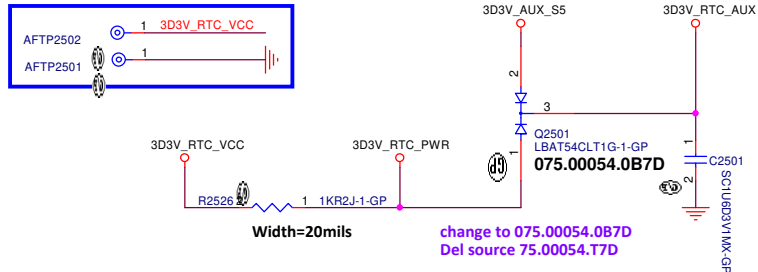
SPI ROM

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SSID = RBATT

Test point



BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title FLASH/RTC			
Size A3	Document Number LS40IC		Rev SC
Date:	Friday, June 14, 2019		Sheet 25 of 106

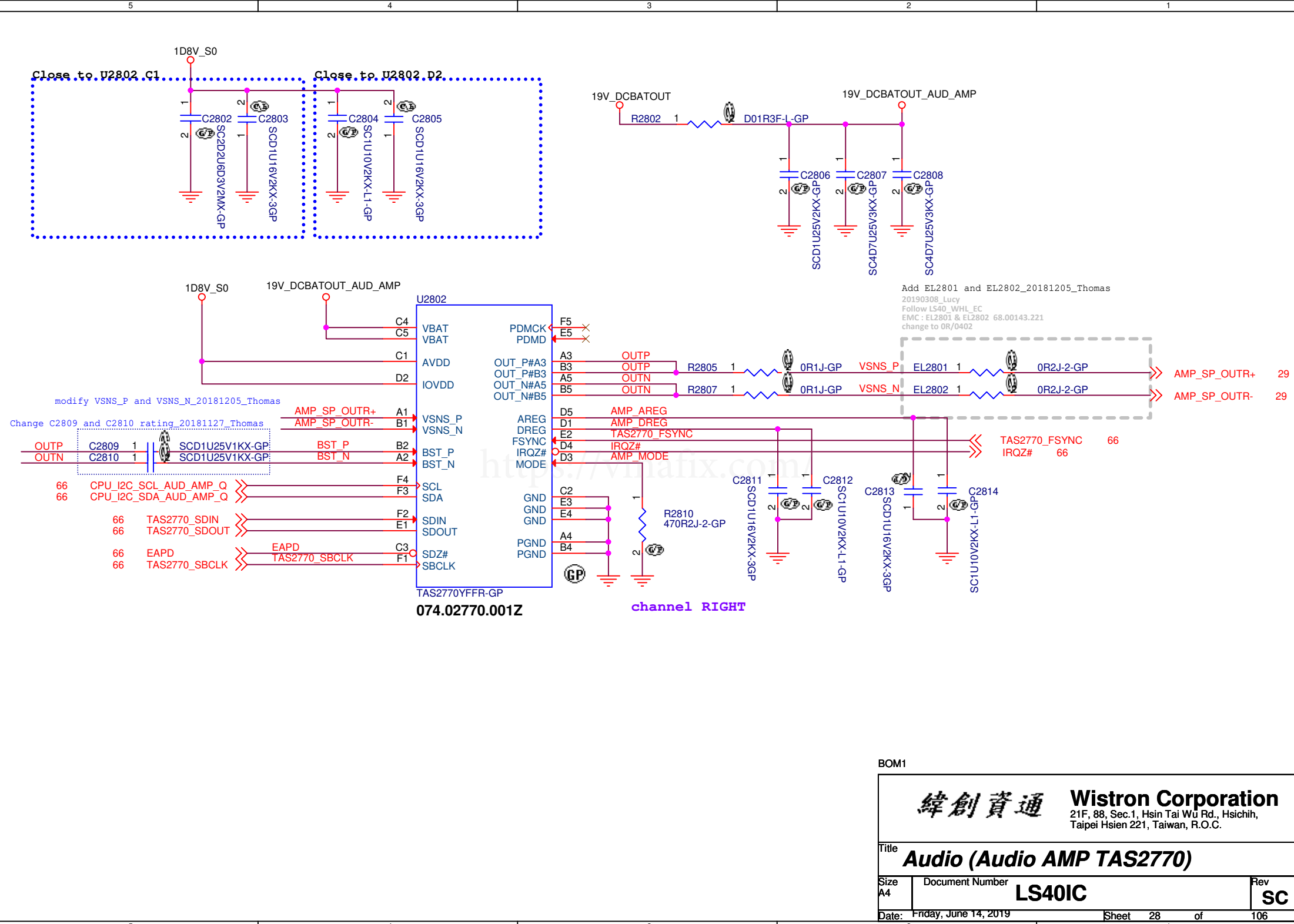


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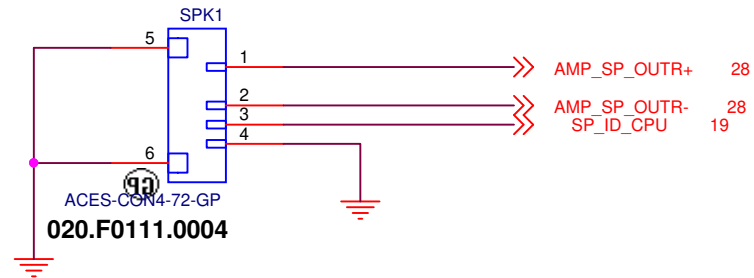
BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Audio (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LS40IC</div>	Rev <div>SC</div>
Date: Friday, June 14, 2019		Sheet 27 of 106



BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Audio (Audio AMP TAS2770)			
Size A4	Document Number LS40IC		Rev SC
Date:	Friday, June 14, 2019	Sheet 28 of	106



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BOM1

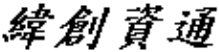
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title Audio (HP/SPK/MIC Jack)	
Size A4	<div>Document Number</div> <div>LS40IC</div>
Date: Friday, June 14, 2019	Sheet 29 of 106

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BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (RSVD			
Size A4	Document Number LS40IC		Rev SC
Date: Friday, June 14, 2019		Sheet 30 of	106

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>LAN (RSVD)</div>	
Size <div>A4</div>	Document Number <div>LS40IC</div>
Date <div>Friday, June 14, 2019</div>	Rev <div>SC</div>
Sheet 31 of 106	

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BOM1

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>LAN (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LS40IC</div>	Rev <div>SC</div>
Date: Friday, June 14, 2019		Sheet 32 of 106

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title CARDREADER (RSVD)		
Size A4	Document Number LS40IC	Rev SC
Date: Friday, June 14, 2019		Sheet 33 of 106

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title USB (RSVD)		
Size A4	Document Number LS40IC	Rev SC
Date: Friday, June 14, 2019		Sheet 34 of 106

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title USB (RSVD)		
Size A4	Document Number LS40IC	Rev SC
Date: Friday, June 14, 2019		Sheet 35 of 106

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BOM1		
USB (RSVD)		
<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>
Title		
036_USB (RSVD)		
Size	Document Number	Rev
A4	LS40IC	SC
Date: Friday, June 14, 2019		Sheet 36 of 106

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title USB (RSVD)		
Size A4	Document Number LS40IC	Rev SC
Date: Friday, June 14, 2019		Sheet 37 of 106

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BOM1

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>USB (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LS40IC</div>	Rev <div>SC</div>
Date: Friday, June 14, 2019		Sheet 38 of 106

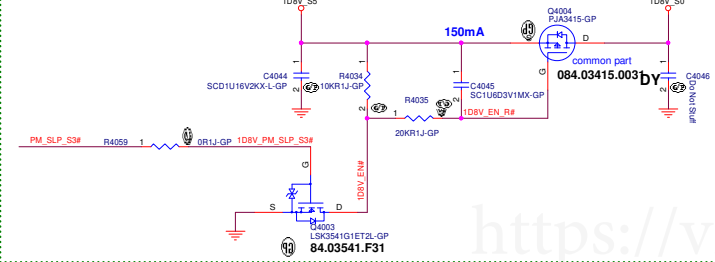
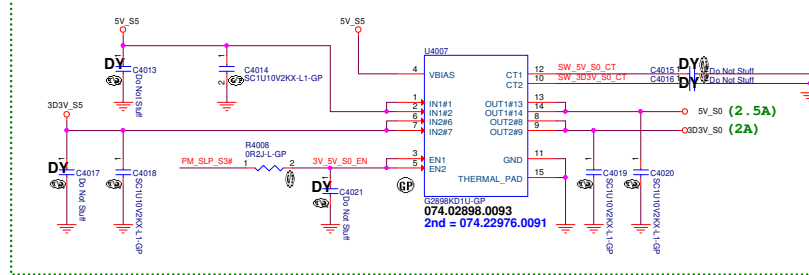
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<https://vinanfx.com/>

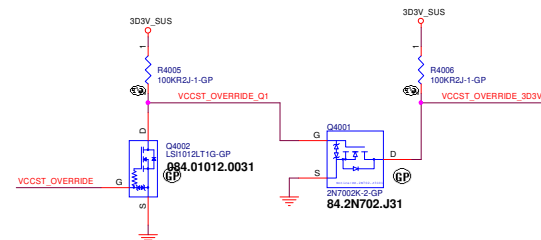
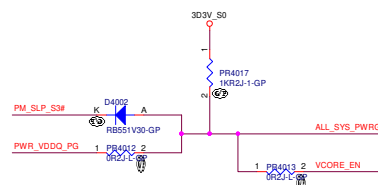
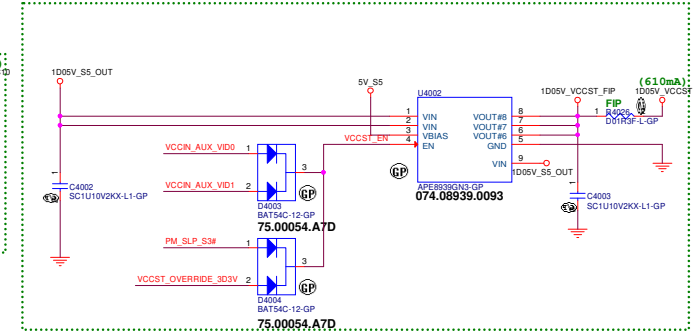
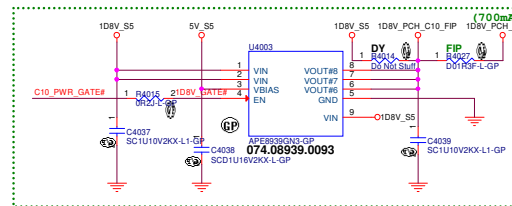
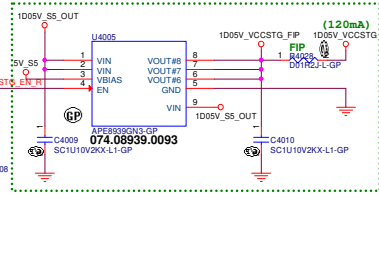
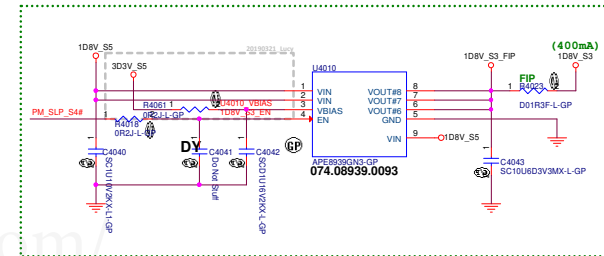
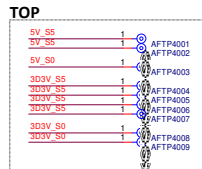
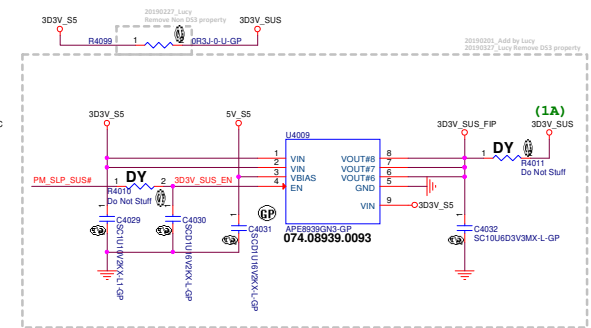
BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Sequence (RSVD)		
Size	Document Number	Rev
A4	LS40IC	SC
Date: Friday, June 14, 2019		Sheet 39 of 106

17	24,51	PM_SLP_S4#	<<>>
17	24,54	PM_SLP_S3#	<<>>
17	24,53	PM_SLP_SUS#	<<>>
17		VCSTC_OVERRIDE	<<>>
17	24	ALL_SYS_PWRGD	<<>>
22	50	VCIN_AUX_VID0	<<>>
22	50	VCIN_AUX_VID1	<<>>
17		PCH_PWROK	<<>>
17		C10_PWR_GATE#	<<>>
46		PWR_VCORE_VR_READY	<<>>
46		PWR_VCORE_VR_EN	<<>>
51		PWR_VDDO_PG	<<>>
	45	3V_5V_EN	<<>>
	24	SS_ENABLE	<<>>



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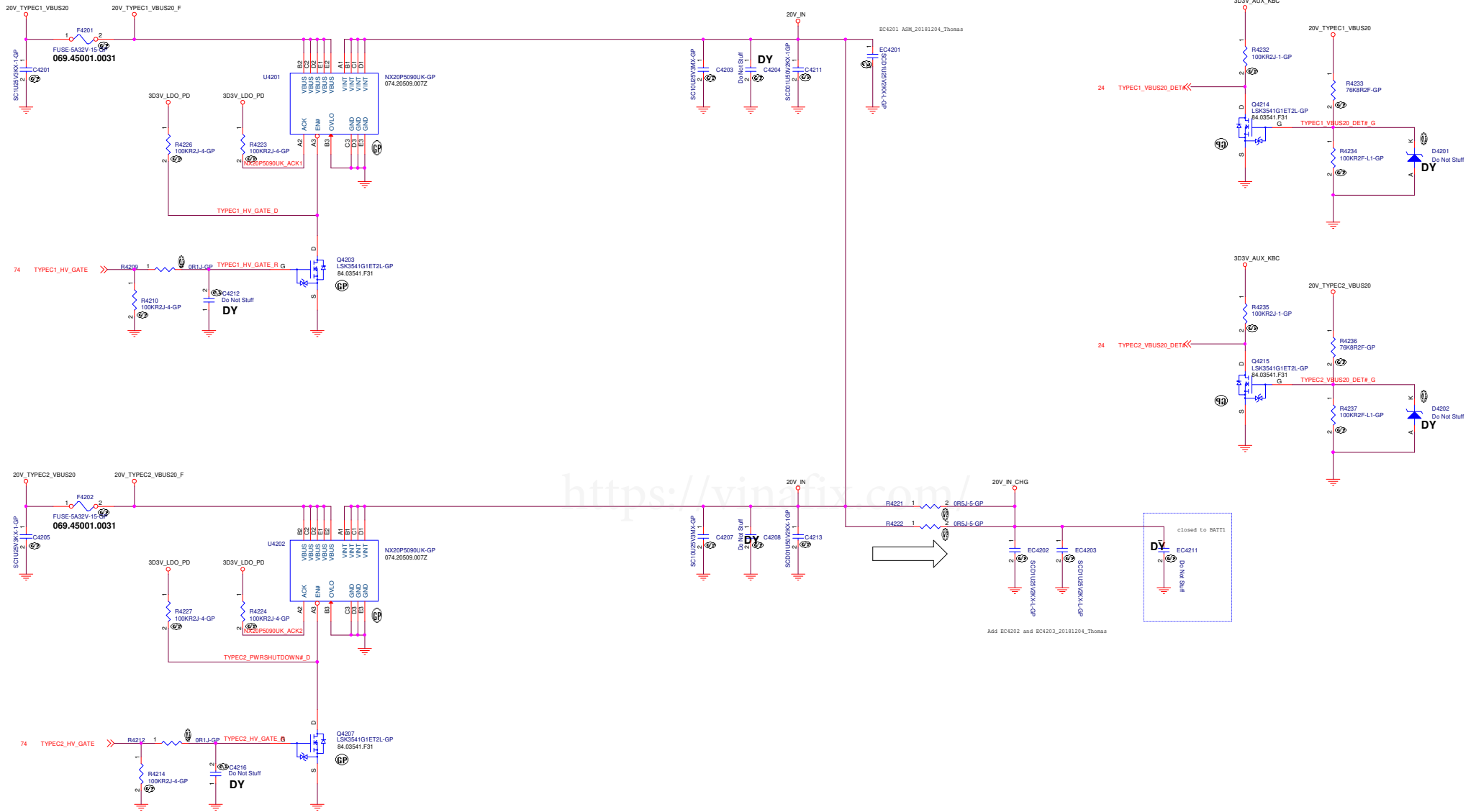
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<https://vinanfx.com/>

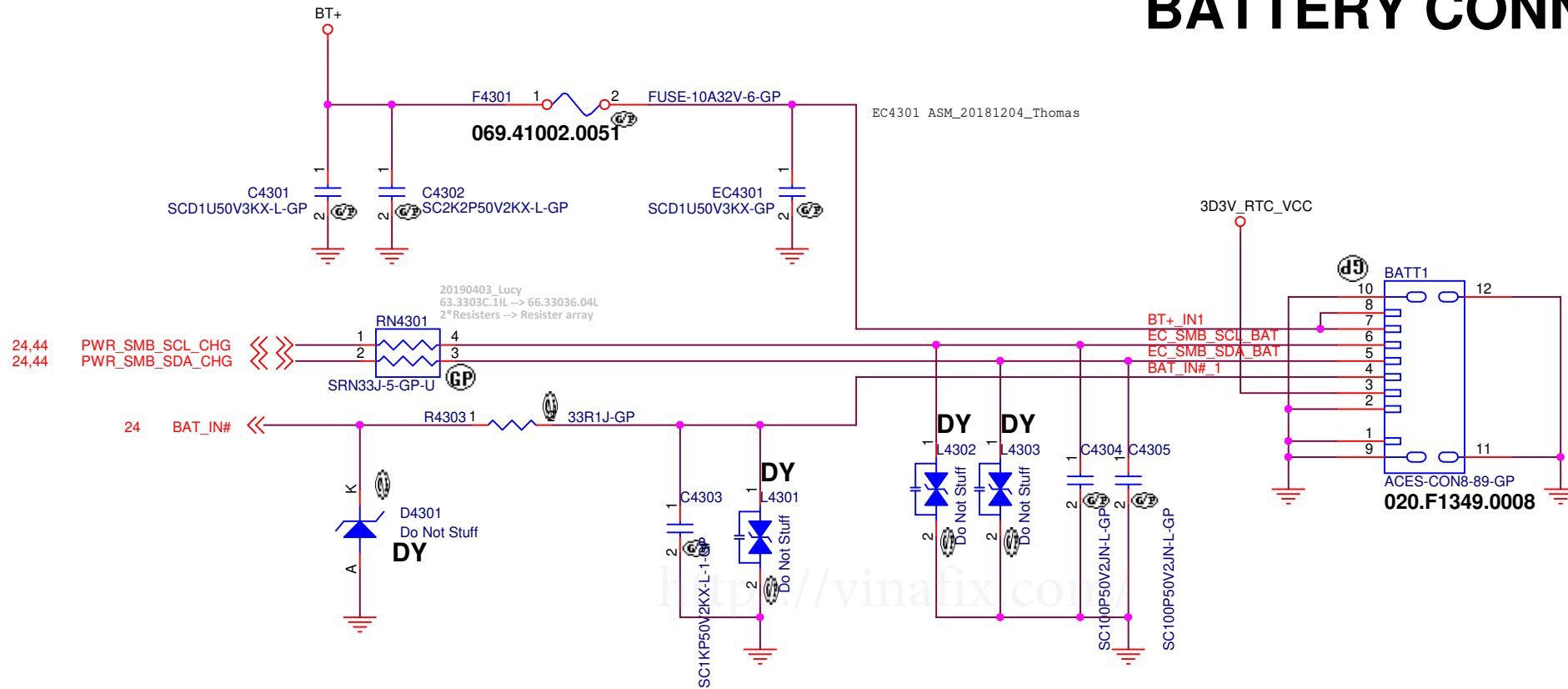
BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Sequence (RSVD)		
Size	Document Number	Rev
A4	LS40IC	SC
Date: Friday, June 14, 2019		Sheet 41 of 106

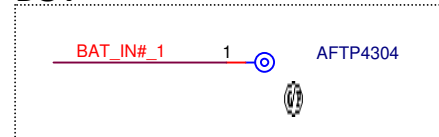
Table
Q4201,Q4202,Q4203,Q4204
1st SI7153DN-T1-GE3 VISHAY
2nd TPC8103 TOSHIBA
Need to apply WPN and symbol
084.08103.M001



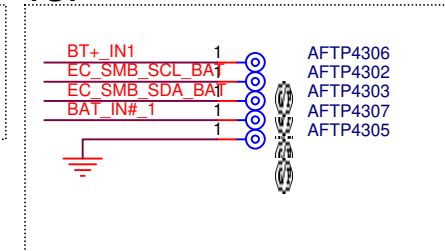
BATTERY CONNECTOR



BOT



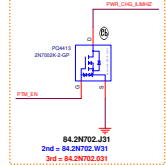
TOP



BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
INT IO (ATX/ DC/ BATT Conn)			
Size	Document Number		Rev
A4	LS40IC		SC
Date:	Friday, June 14, 2019	Sheet 43 of	106

24.43	PWR_SMB_SCL_CHG	»»	PWR_SMB_SCL_CHG
24.43	PWR_SMB_SDA_CHG	»»	PWR_SMB_SDA_CHG
3.24.46	PROCHOT7_CPU	»»	PROCHOT7_CPU
46	CHGR_PSVS_BMP	»»	CHGR_PSVS_BMP
24	PWR_AC_IN	»»	PWR_AC_IN
24	PWR_CHG_MON	»»	PWR_CHG_MON
24	PTM_EN	»»	PTM_EN



Device will be transition from normal **Flash-Boot** operation to **PTM** operation by:

- Set REG0x0217 = 0, to disable the **PTM_EXTMEM**.
- Set REG0x0208 = 1.
- Set REG0x0202 = 1.
- Ground **LUM_HZ** pin.

Device will transition out of **PTM** mode with host control by:

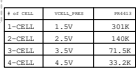
- Set REG0x0202 = 0.
- Pull **LUM_HZ** pin to high.

Device exits **PTM** flash-boost operation if tripping **VDDPWR** or **REGPWR**.

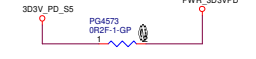
- Device exits **PTM** flash-boost operation under fault conditions (**SDOC**, **TBRU**, **BATCON**).

Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	110K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

0505
buyer: 7"



OFFPAGE-GAP



OFFPAGE
Check PIC-EE

3,24	PROCHOT0_CPU	<<	PROCHOT0_CPU
	7 SVID_CLK_CPU	<<	SVID_CLK_CPU
	7 SVID_DATA_CPU	<<	SVID_DATA_CPU
	7 SVID_ALERT0_CPU	<<	SVID_ALERT0_CPU
40	PWR_VCORE_VR_EN	<<	PWR_VCORE_VR_EN
47	PWR_VCORE_PWM1	<<	PWR_VCORE_PWM1
47	PWR_VCORE_PWM2	<<	PWR_VCORE_PWM2
47	PWR_VCORE_PWM3	<<	PWR_VCORE_PWM3
40	PWR_VCORE_VR_READY	<<	PWR_VCORE_VR_READY
	47 PWR_VCORE_TEMP	<<	PWR_VCORE_TEMP
47	PWR_VCORE_STB	<<	PWR_VCORE_STB
	47 PWR_VCORE_CS1	<<	PWR_VCORE_CS1
	47 PWR_VCORE_CS2	<<	PWR_VCORE_CS2
	47 PWR_VCORE_CS3	<<	PWR_VCORE_CS3
7	VCCORE_SENSE	<<	VCCORE_SENSE
7	VSSCORE_SENSE	<<	VSSCORE_SENSE
44	CHGR_PSYS_MVP	<<	CHGR_PSYS_MVP

20,24 EC_I2C_SCL4 <<>> PR4680 1 DY Do Not Stuff PWR_VCORE_SCL_P_EC

20,24 EC_I2C_SDA4 <<>> PR4681 1 DY Do Not Stuff PWR_VCORE_SDA_P_EC



Reserve for Power test

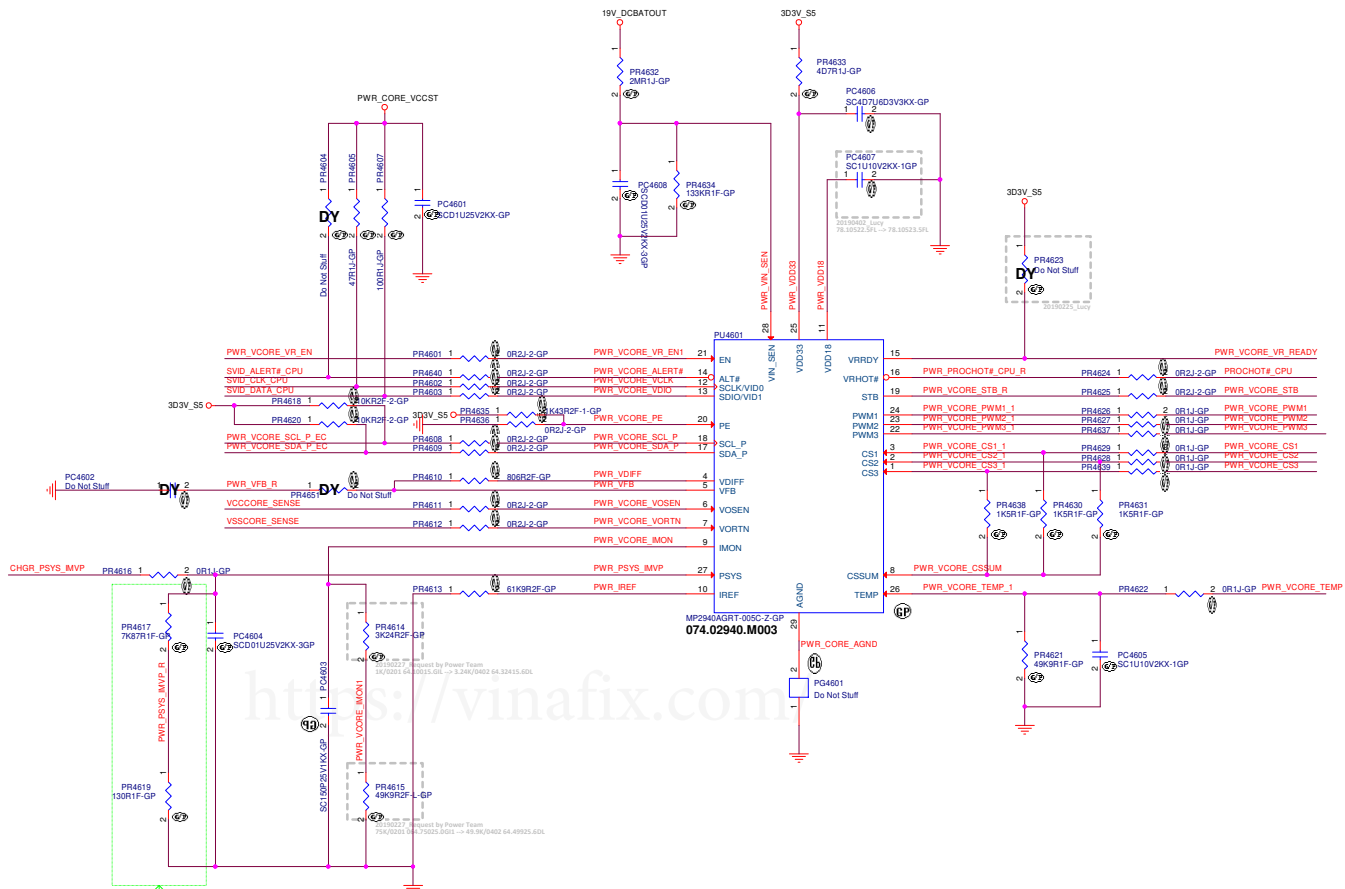
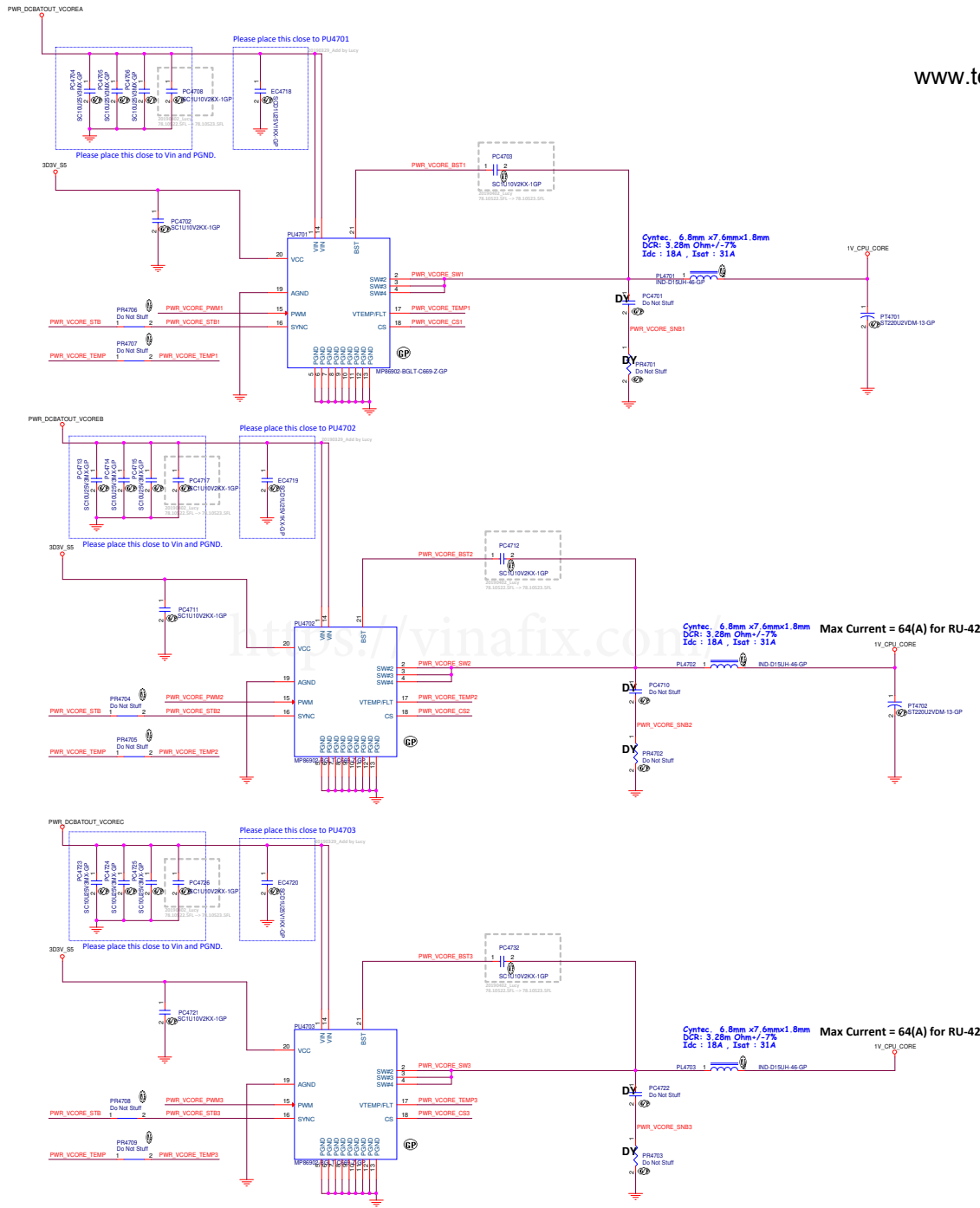
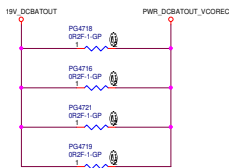
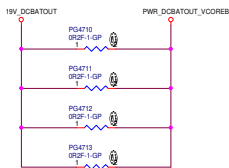
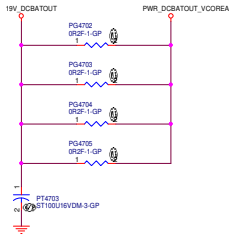


TABLE : PSYS Pull Down Resistor (RPSYS)

ADC VREF	IPSYS	PSYS_PMAX	RPSYS
0.8V	1uA/W	100W	8K-ohm

46	PWR_VCORE_TEMP	>>	PWR_VCORE_TEMP
46	PWR_VCORE_STB	>>	PWR_VCORE_STB
46	PWR_VCORE_CS1	>>	PWR_VCORE_CS1
46	PWR_VCORE_CS2	>>	PWR_VCORE_CS2
46	PWR_VCORE_CS3	>>	PWR_VCORE_CS3
46	PWR_VCORE_PWM1	>>	PWR_VCORE_PWM1
46	PWR_VCORE_PWM2	>>	PWR_VCORE_PWM2
46	PWR_VCORE_PWM3	>>	PWR_VCORE_PWM3



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Title POWER (RSVD)		
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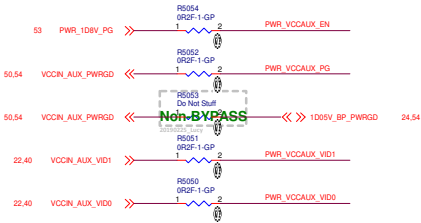
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Title POWER (RSVD)		
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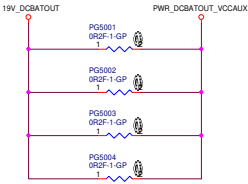


TABLE: MP2941 VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

← LOGIC

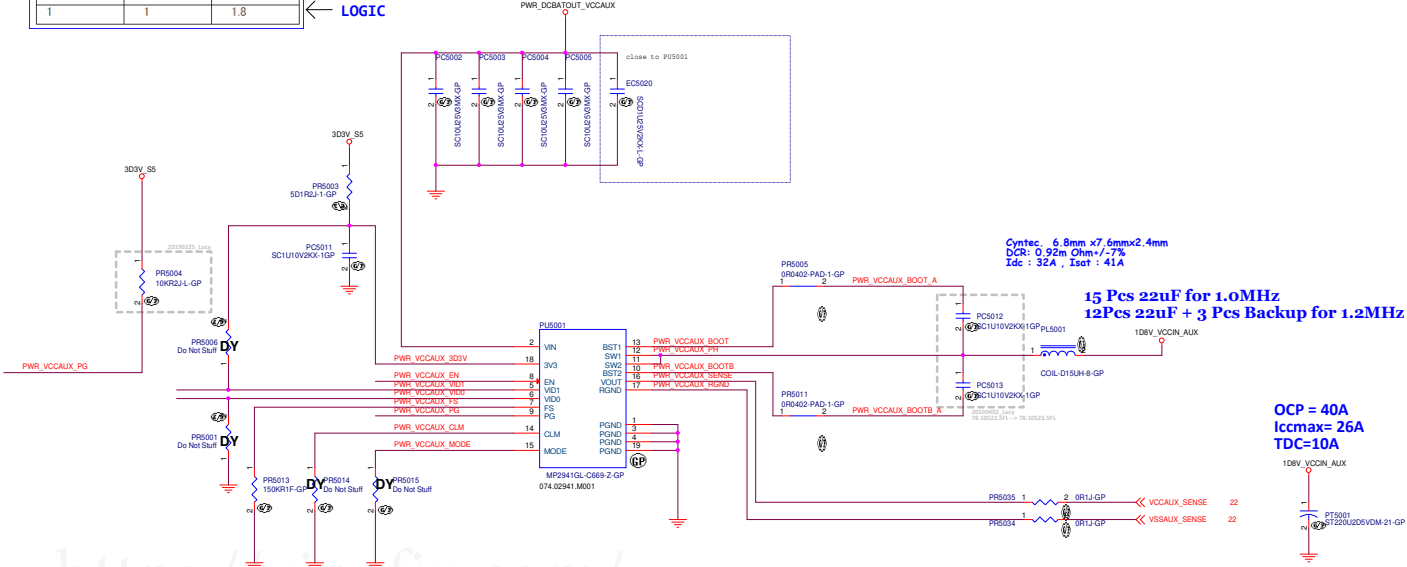


TABLE: MP2941 FS Selection

RMode	Fs
0	500kHz
90.9K	700kHz
150K	1000kHz
>230K or float	1200kHz

← LOGIC

TABLE: MP2941 CLM/Phase Selection

RCLM	CLM
0	7A
90.9K	10A
150K	13A
>230K or float	16A

← LOGIC

TABLE: MP2941 Mode Selection

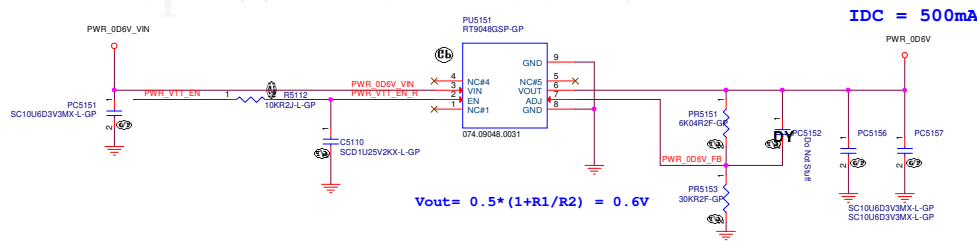
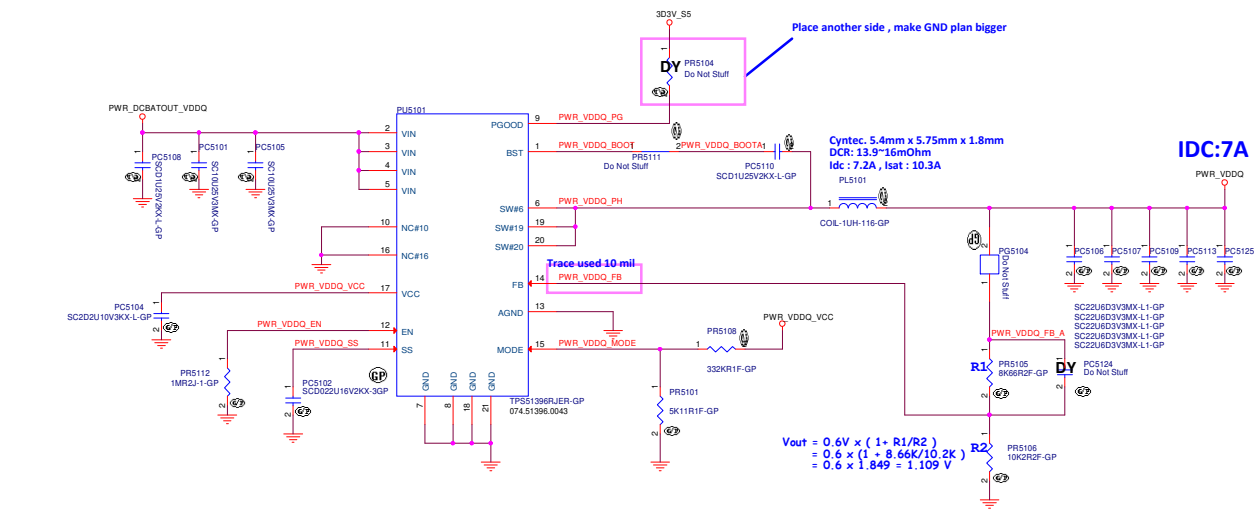
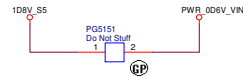
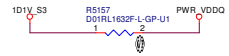
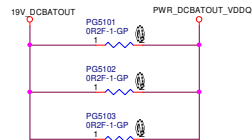
RMode	Interleaving	VID Down
0	N	Slew down
90.9K	Y	Slew down
150K	Y	Decay
>230K or float	N	Decay

← LOGIC

TABLE : MP2941

Item	R0 sample	R1 sample
VOUT	1.65V fixed	Defined by VCCPCHCORE_VID1/VID0
RMode	0 ohm	Float
RFS	Float	Float or 150K
1Kohm bleeder	Necessary	Not necessary

The diagram shows the timing relationship between the PM_SLP_S4# signal and the power management signals PWR_VDDQ_PG, PWR_VDDQ_EN, and PWR_VTT_EN. The PM_SLP_S4# signal is shown as a pulse from 17.24.40.51 to 40.51. The PWR_VDDQ_PG signal is shown as a pulse from 40.51 to 40.51. The PWR_VDDQ_EN and PWR_VTT_EN signals are shown as pulses from 17.24.40.51 to 40.51. The diagram is divided into two sections by a dashed line. The top section shows the PM_SLP_S4# signal and the PWR_VDDQ_PG signal. The bottom section shows the PM_SLP_S4# signal and the PWR_VDDQ_EN and PWR_VTT_EN signals. The signals are labeled with their respective pin numbers and functions: RS110 (PWR_VDDQ_PG), RS111 (PWR_VTT_EN), and RS113 (PWR_VTT_EN). The signals are also labeled with their respective functions: PWR_VDDQ_PG, PWR_VDDQ_EN, and PWR_VTT_EN. The signals are shown as pulses with a duration of 100ns.

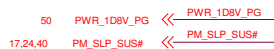


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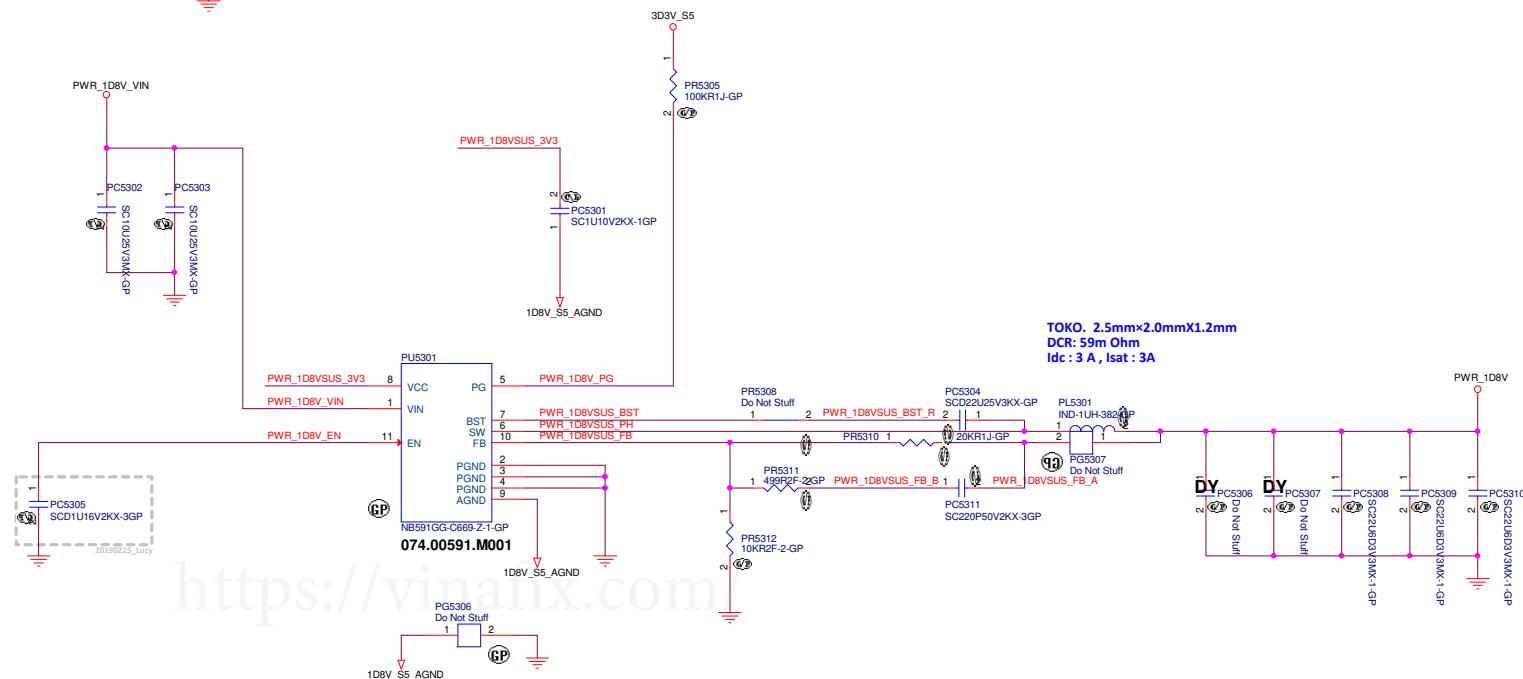
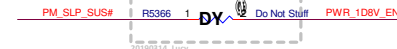
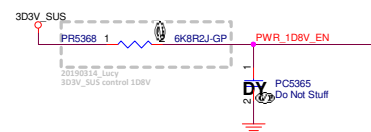
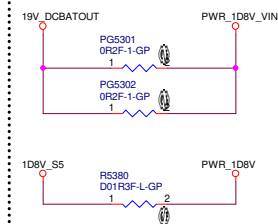
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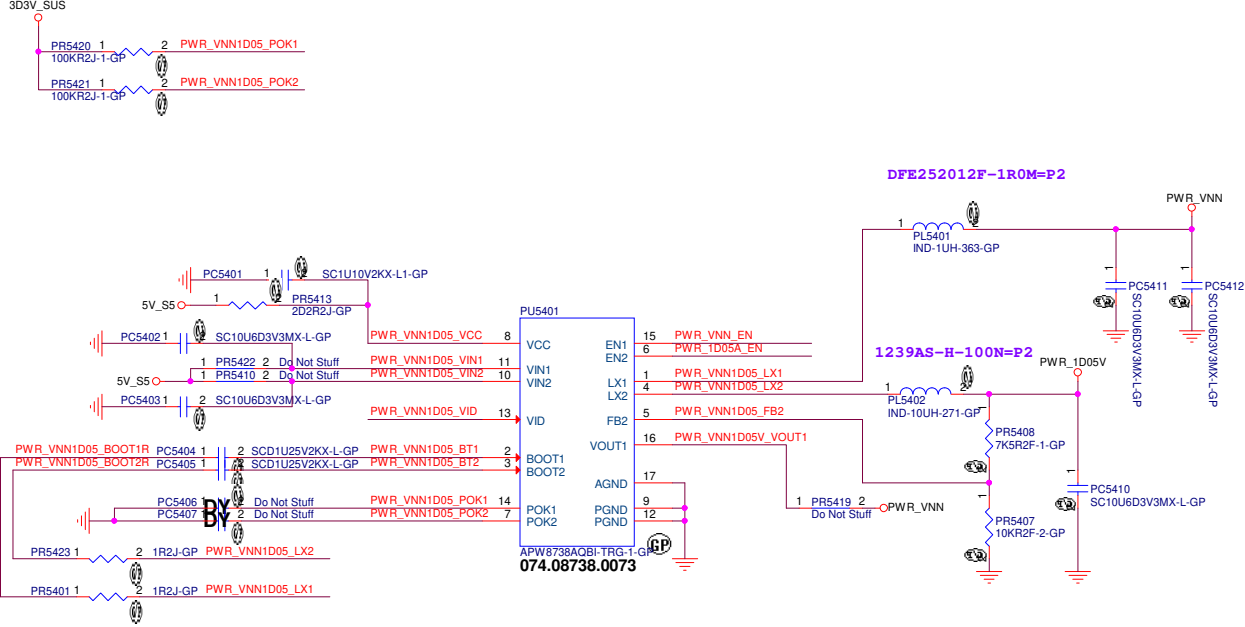
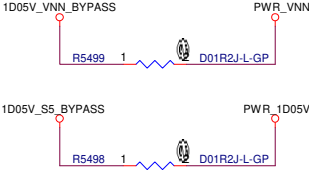
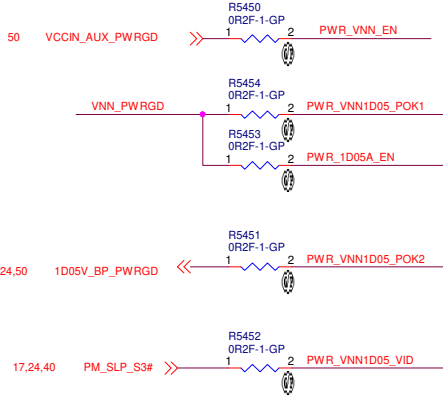
Title **POWER (NB591/1D8V)**

Size Custom	Document Number LS40IC	Rev S
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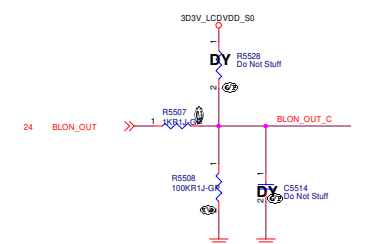
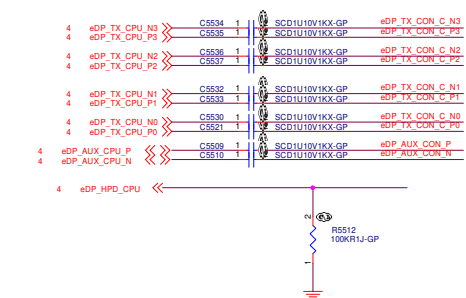
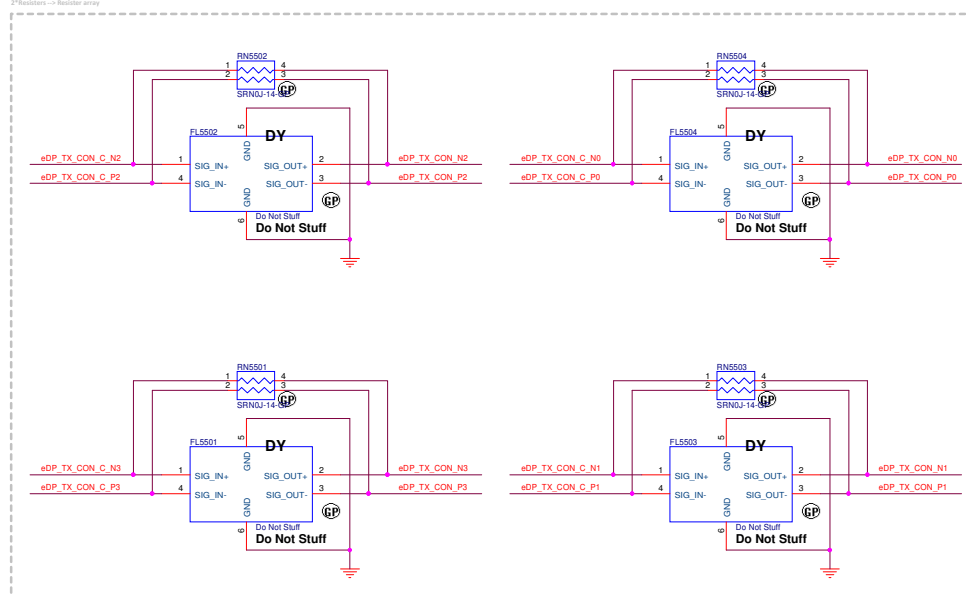
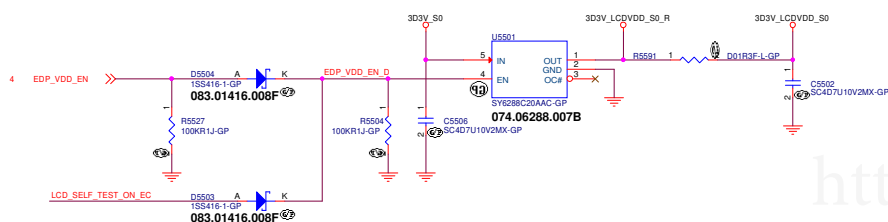
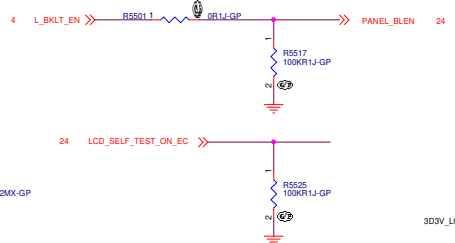
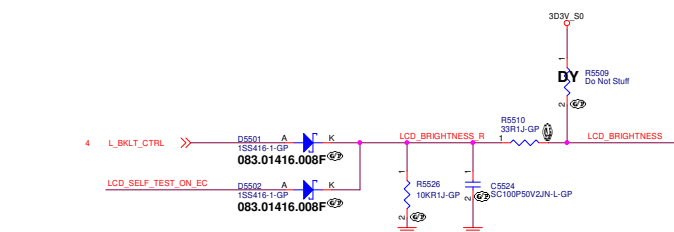
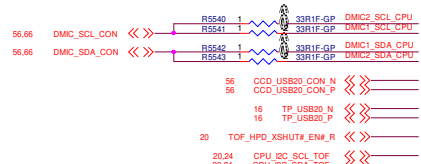
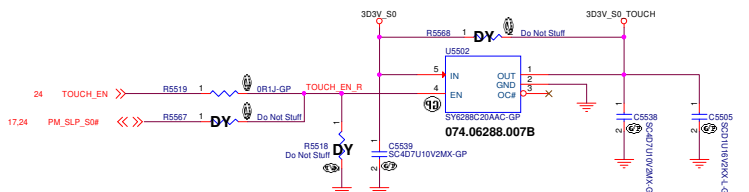
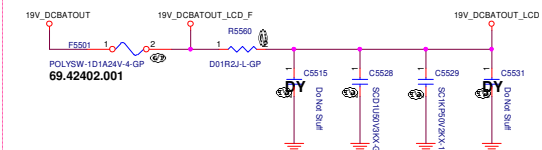


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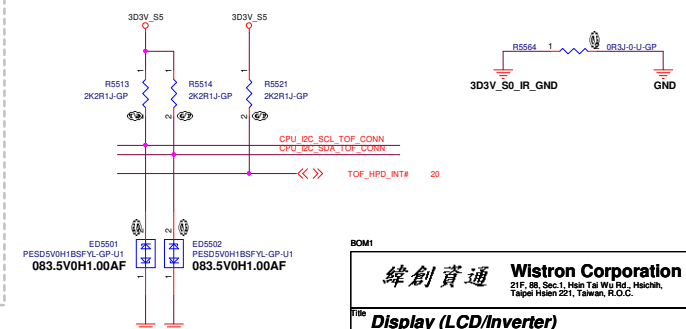
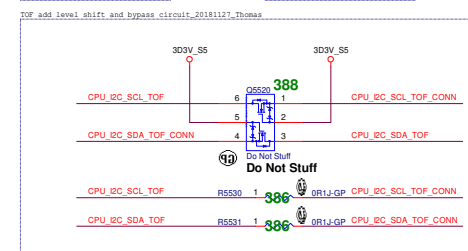
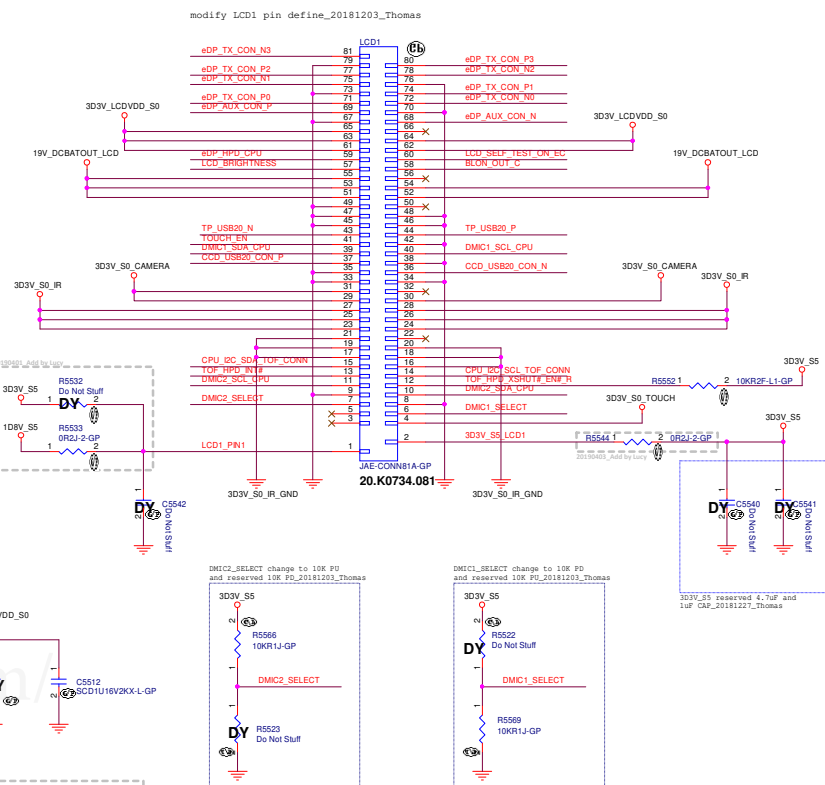
緯創資通 Wistron Corporation		
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Title POWER(APW8738A_VNN1D05)		
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Main Func = LCD

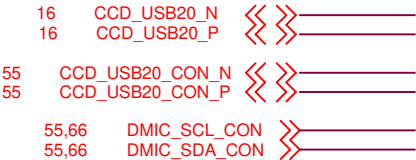
INVERTER POWER



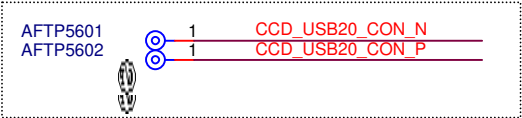
LCD Connector



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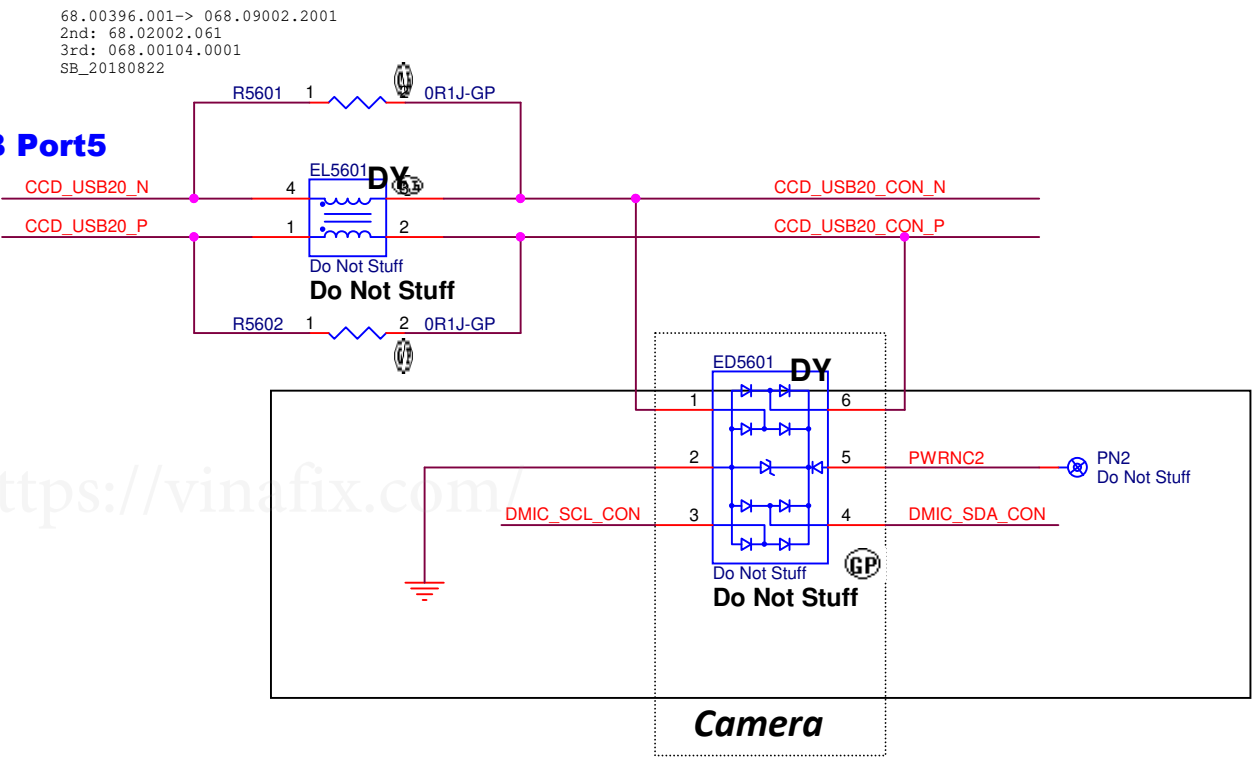


TOP



CCD CONN

CAMERA_USB Port5



BOM1

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Title			
Display (CRT/IR Camera)			
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Title Display (RSVD)		
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Title Display (RSVD)		
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Title		
Display (RSVD)		
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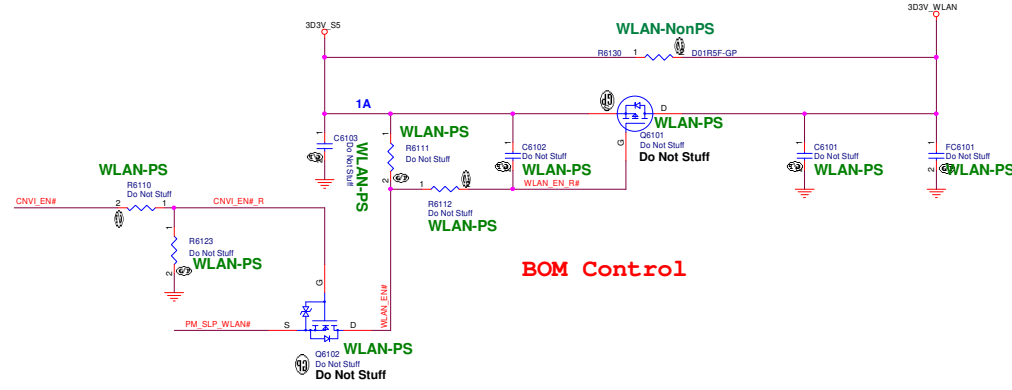
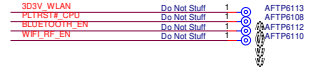
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
INT IO (RSVD)			
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Main Func = WLAN

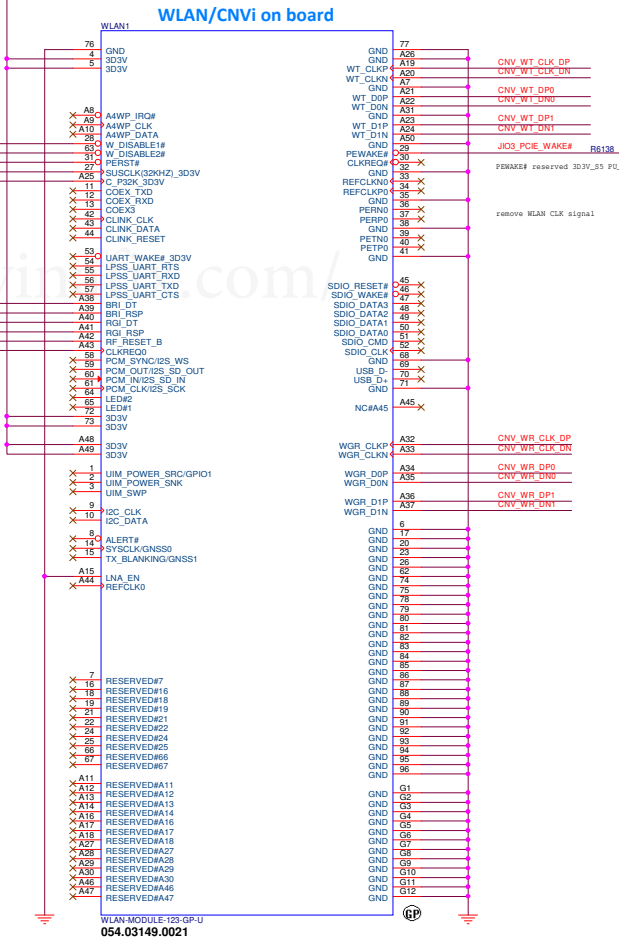
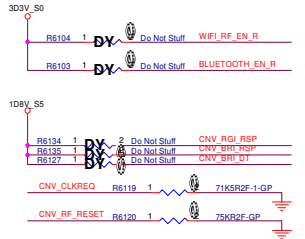
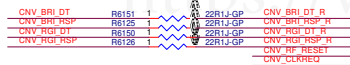
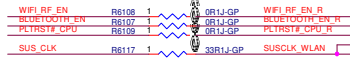
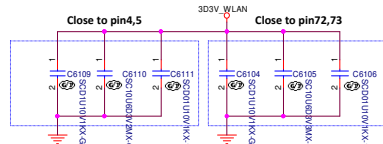
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19	CNV_CLKREQ	Do Not Stuff	1	AFTP6108
19	CNV_RF_RESET	Do Not Stuff	1	AFTP6112
3	CNV_EN#	Do Not Stuff	1	AFTP6110
20,24	WiFi RF_EN	Do Not Stuff	1	
17,24,26,63,7,172	PLTRST#_CPU	Do Not Stuff	1	
18	SUS_CLK	Do Not Stuff	1	
21	CNV_BRI_DT	Do Not Stuff	1	
21	CNV_RGI_RSP	Do Not Stuff	1	
15,21	CNV_RGI_DT	Do Not Stuff	1	
21	CNV_WT_CLK_DP	Do Not Stuff	1	
21	CNV_WT_CLK_DN	Do Not Stuff	1	
21	CNV_WT_DP0	Do Not Stuff	1	
21	CNV_WT_DN0	Do Not Stuff	1	
21	CNV_WT_DP1	Do Not Stuff	1	
21	CNV_WT_DN1	Do Not Stuff	1	
21	CNV_WR_CLK_DP	Do Not Stuff	1	
21	CNV_WR_CLK_DN	Do Not Stuff	1	
21	CNV_WR_DP0	Do Not Stuff	1	
21	CNV_WR_DN0	Do Not Stuff	1	
21	CNV_WR_DP1	Do Not Stuff	1	
21	CNV_WR_DN1	Do Not Stuff	1	
17	PM_SLP_WLAN#	Do Not Stuff	1	



BOM Control

C6110 change size to 0402_20181203_Thomas



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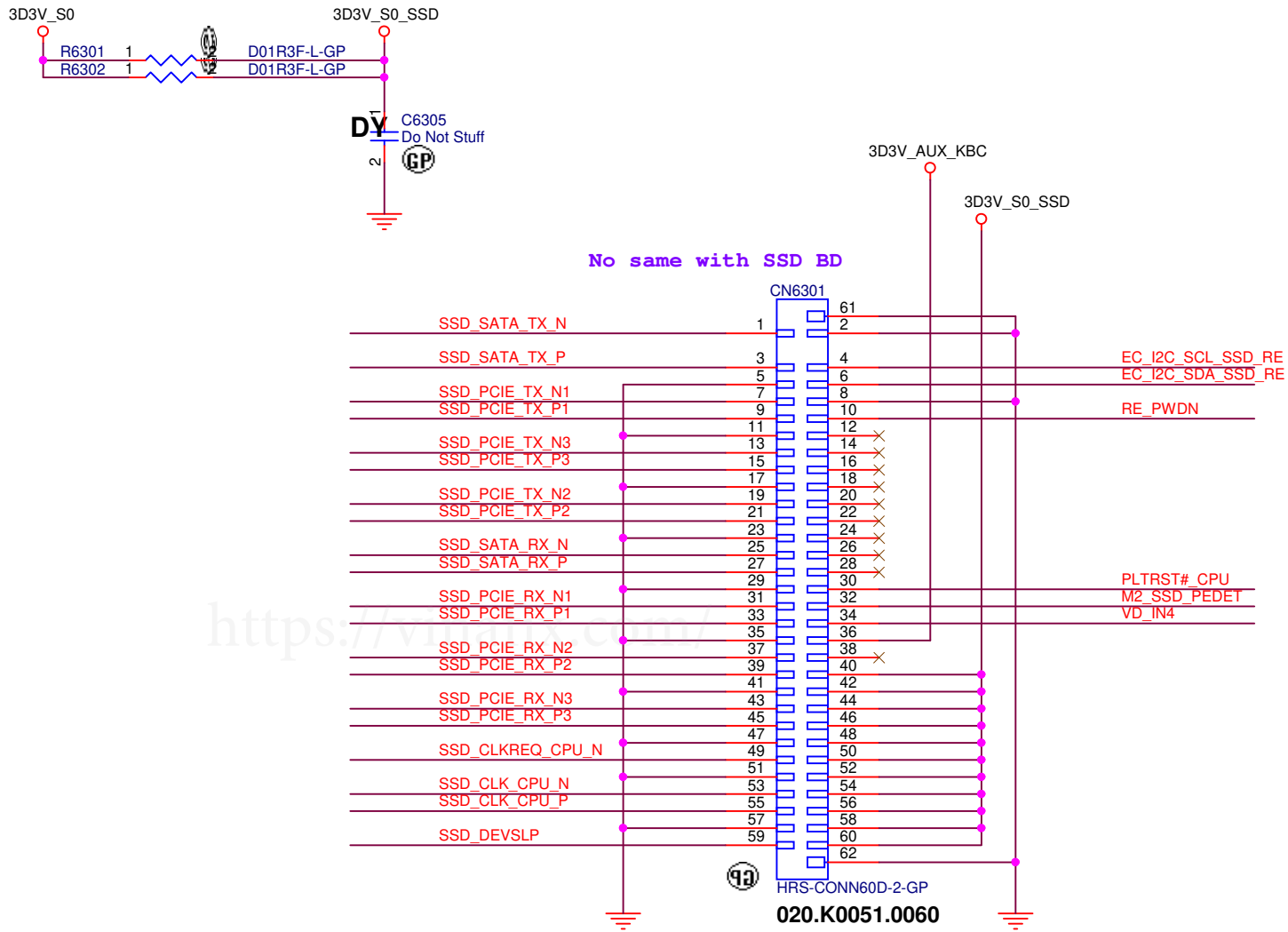
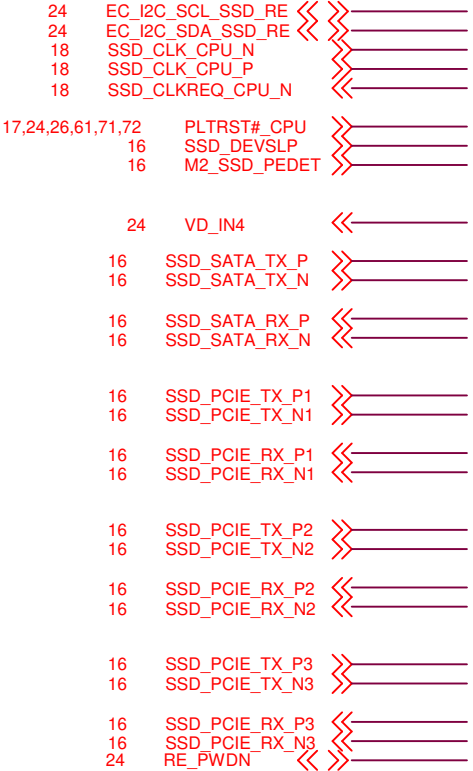
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Title INT IO (RSVD)		
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SSD CONN

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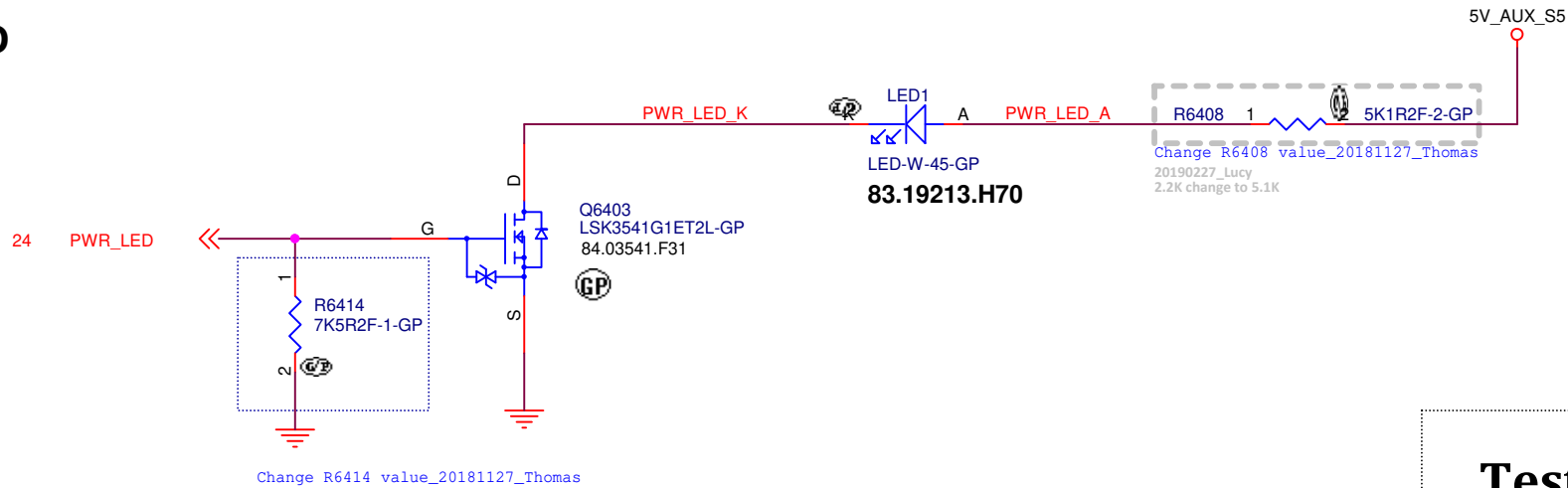


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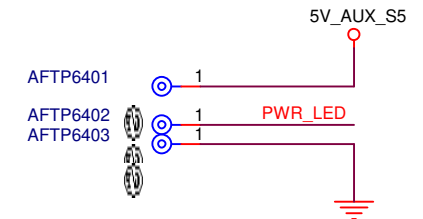
緯創資通 Wistron Corporation	
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Title INT IO (SSD M.2/ eMMC)	
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LED

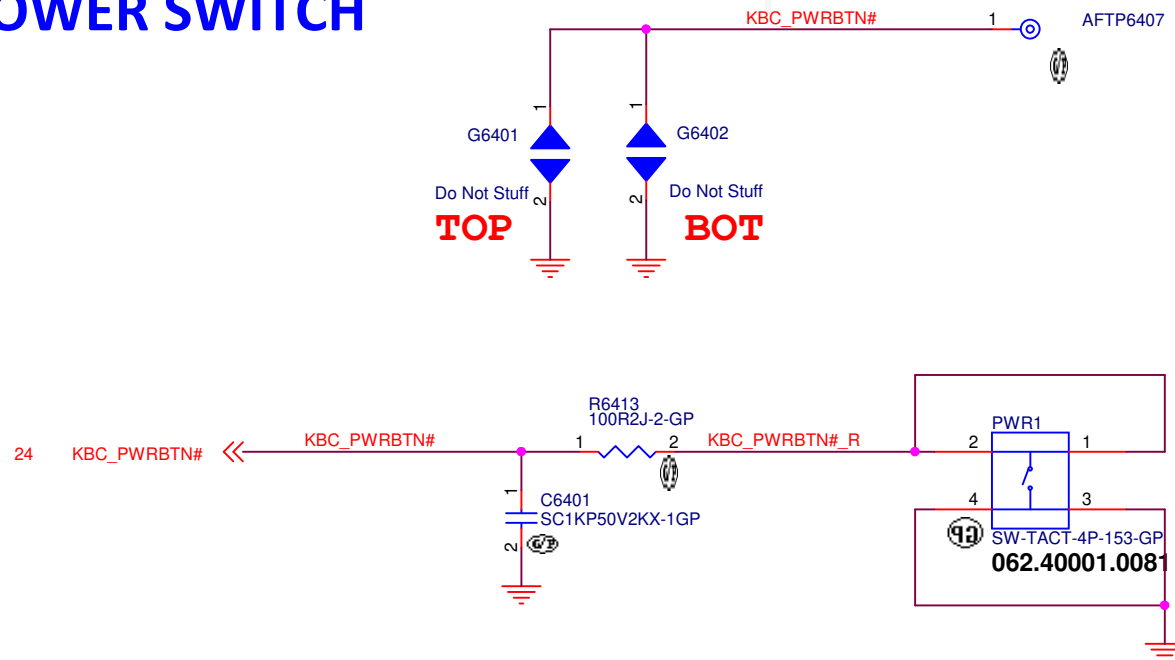
PWR LED



Test point



KBC_PWRBTN# POWER SWITCH



BOM1

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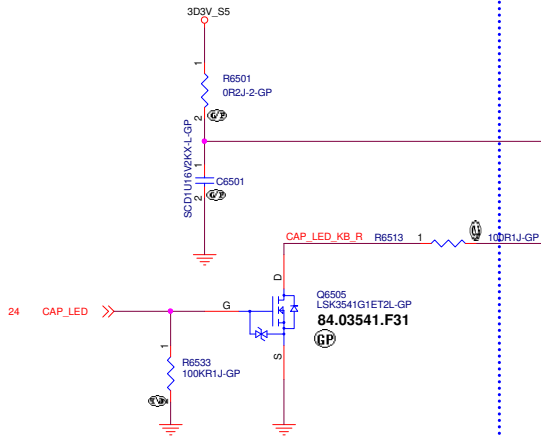
Title **LED / Power Button / NOVO**

Size A4 Document Number **LS40IC** Rev **SC**

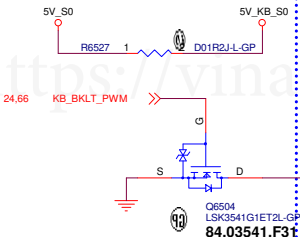
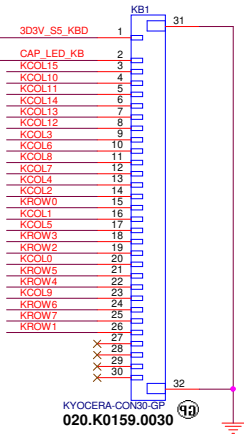
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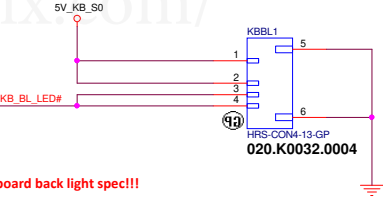
24 KCOL[15:0] >>
24 KROW[7:0] <<



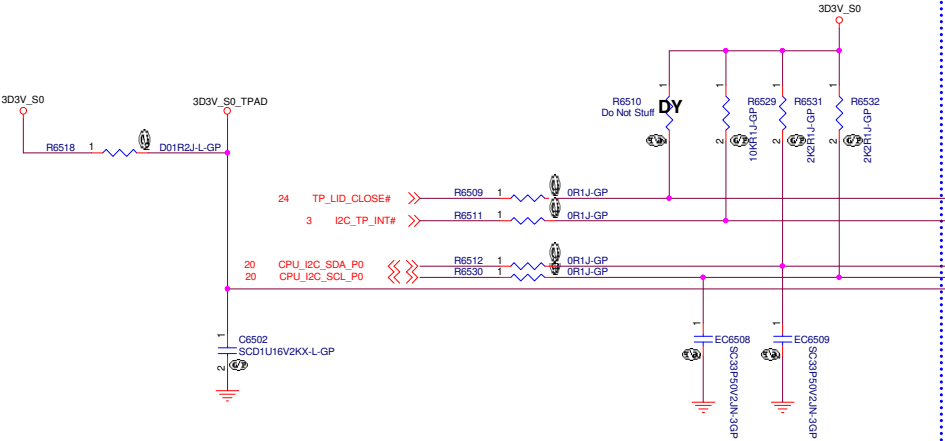
KB CONN



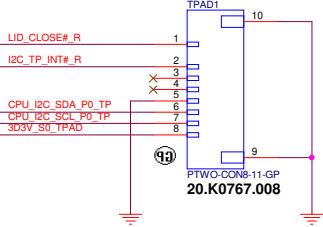
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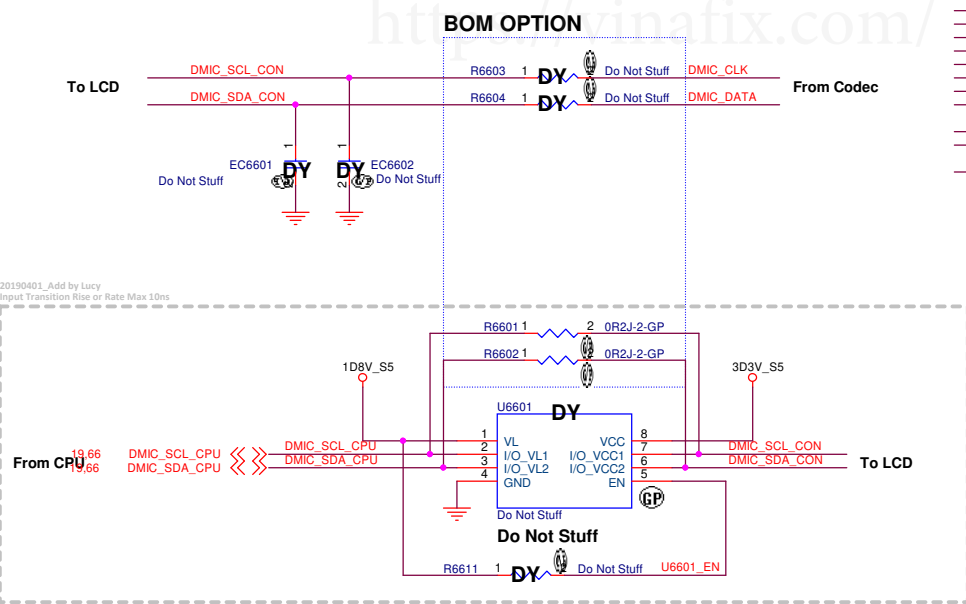
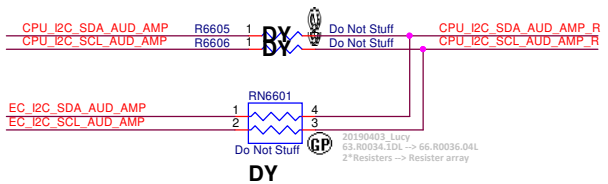
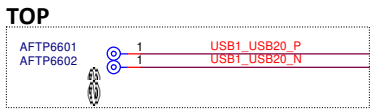
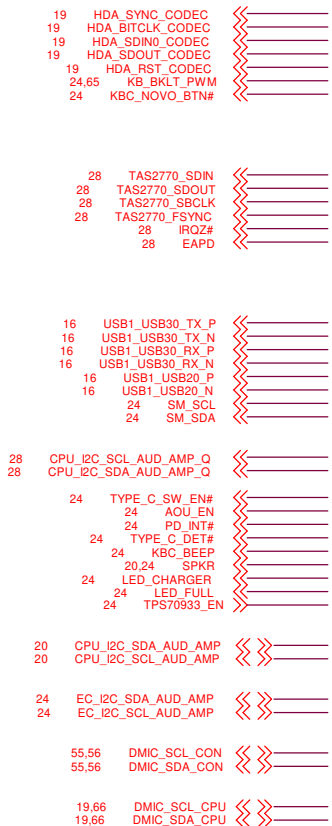
Neek to check keyboard back light spec!!!
De! KBB1_DEFINE1 R6505 100R to KBC
De! KBB1_DEFINE2 R6534 OR to GND



TPAD CONN

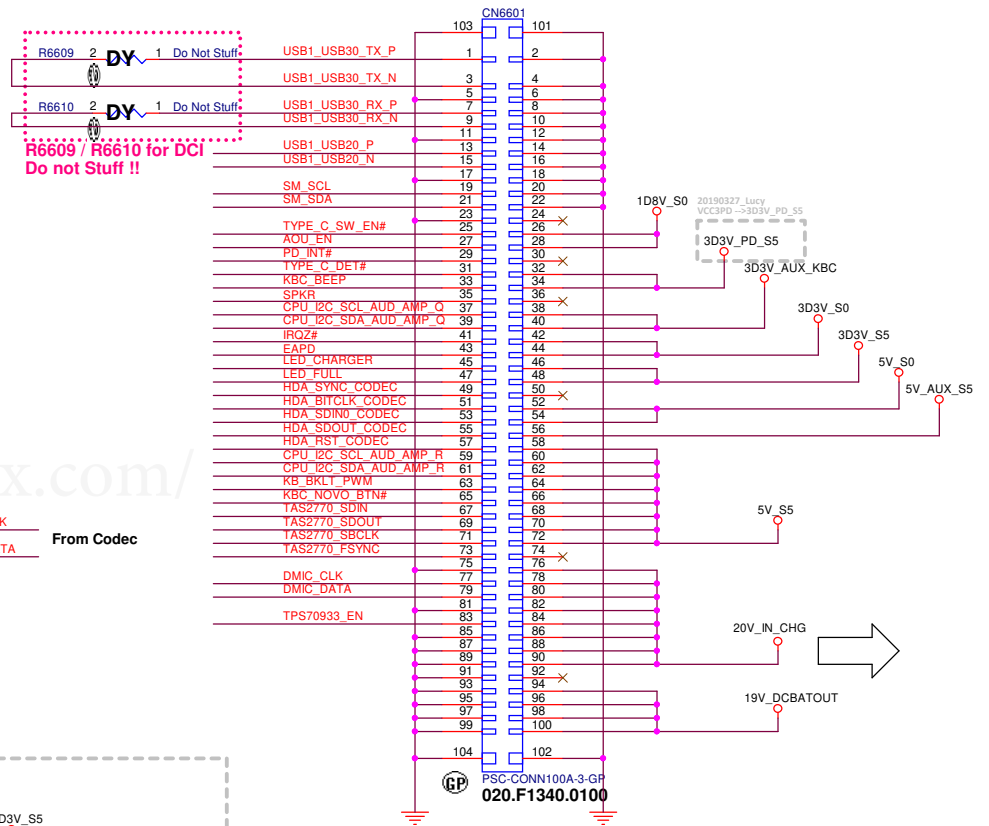


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TO IOBD CONN

modify CN6601 pin define_20181127_Thomas



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IO Board Conn (TYPEC/AUDIO)

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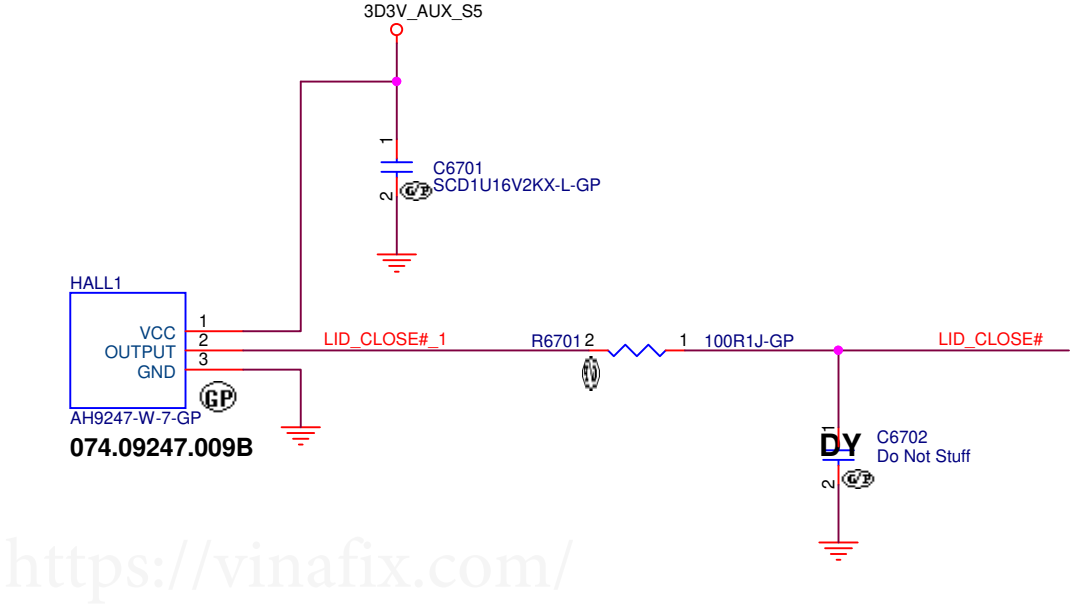
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24 LID_CLOSE# <<—

HALL SENSOR

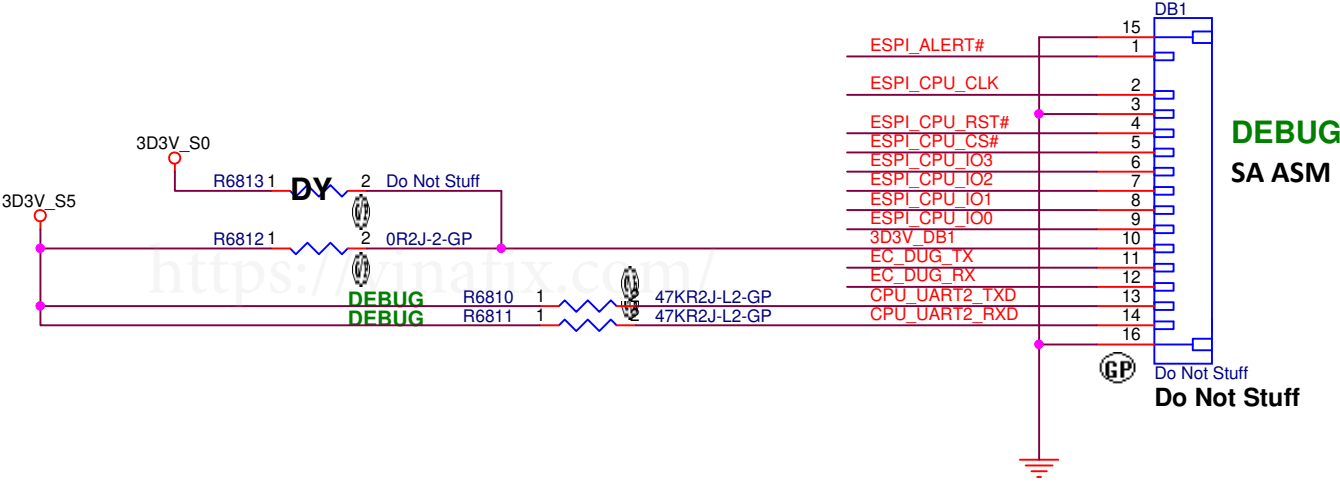


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20	CPU_UART2_TXD	<<<>>>	
20	CPU_UART2_RXD	<<<>>>	
24	ESPI_ALERT#	<<<>>>	
18,24	ESPI_CPU_CLK	<<<>>>	
18,24	ESPI_CPU_RST#	<<<>>>	
24	EC_DUG_RX	<<<>>>	
24	EC_DUG_TX	<<<>>>	
18,24	ESPI_CPU_CS#	<<<>>>	
18,24	ESPI_CPU_IO3	<<<>>>	
18,24	ESPI_CPU_IO2	<<<>>>	
18,24	ESPI_CPU_IO1	<<<>>>	
18,24	ESPI_CPU_IO0	<<<>>>	



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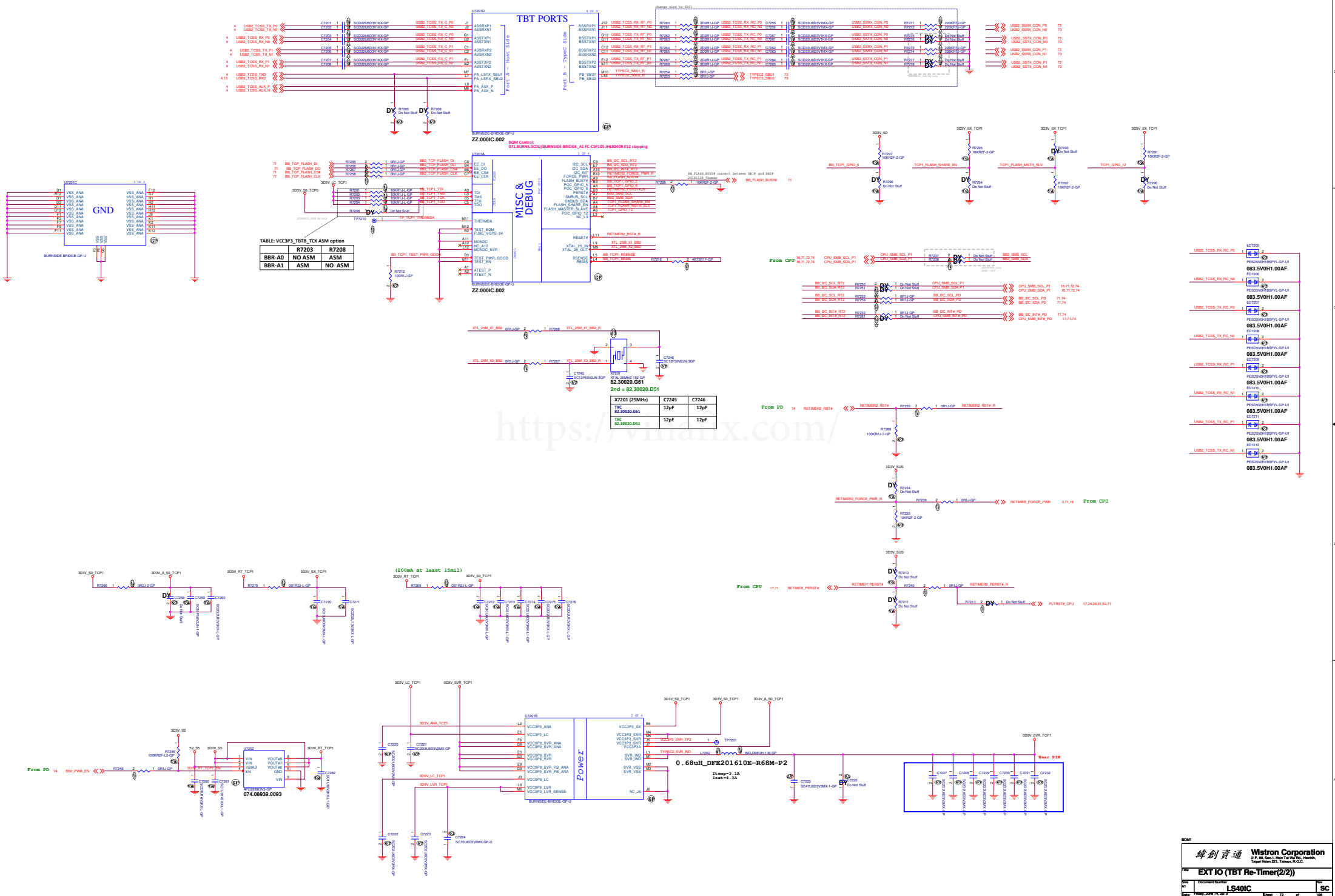
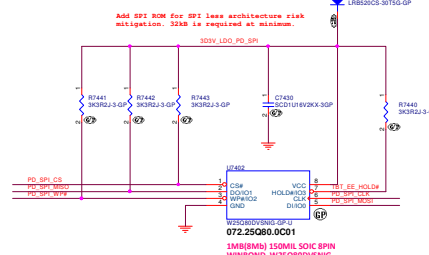
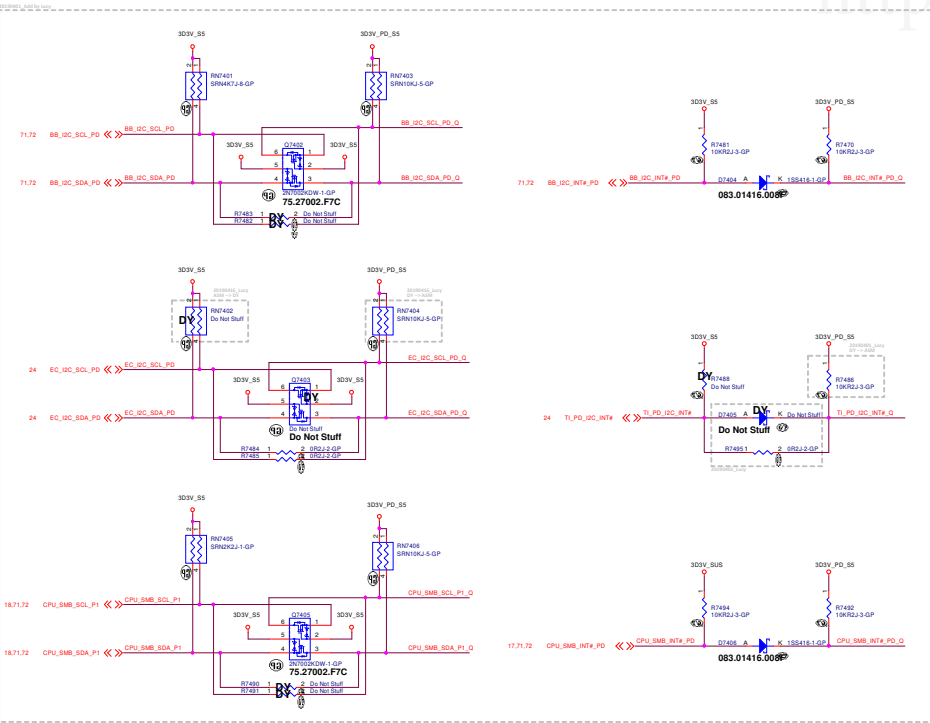
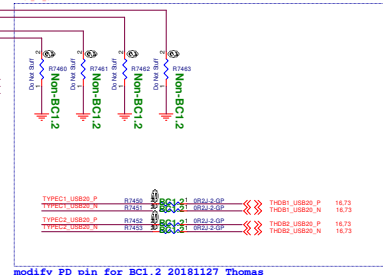
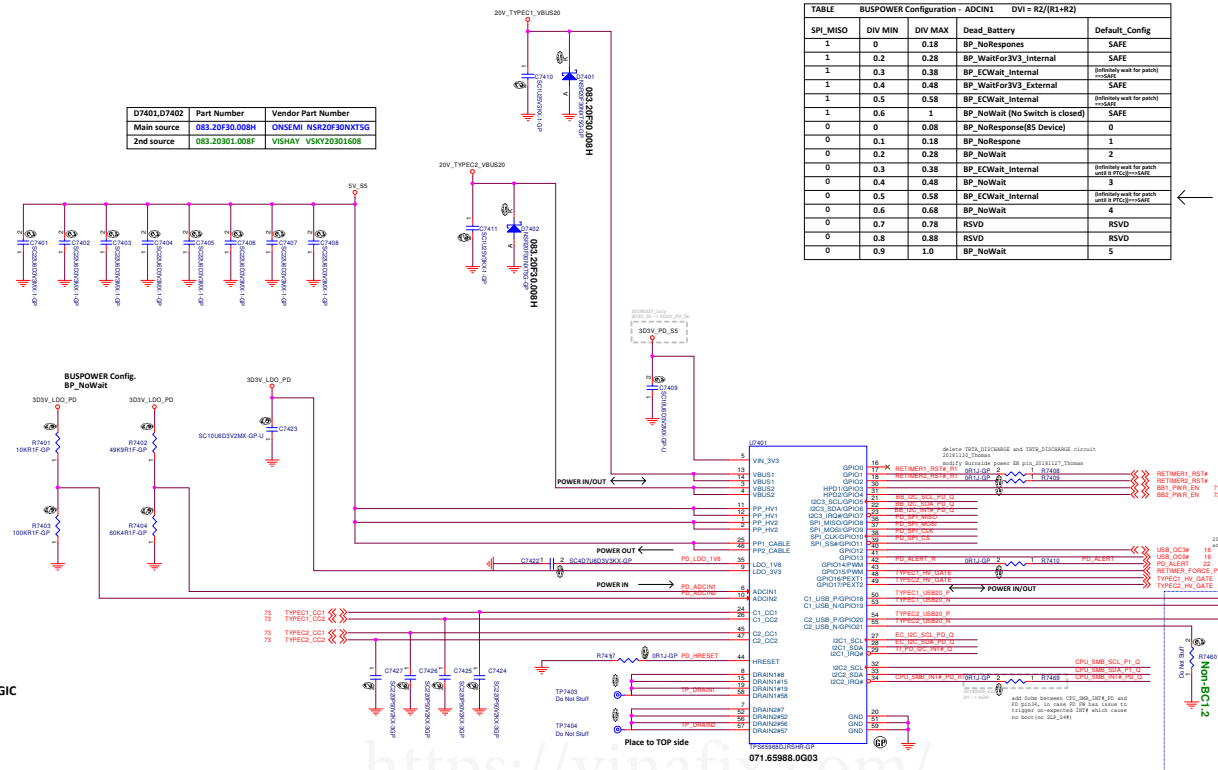




TABLE	BUSPUPON Configuration - ADCIN1				DVI = R2/R1+R2	
SPR_MISO	DIV MIN	DIV MAX	Dead_Battery		Default_Config	
1	0	0.18	BP_NoResponse		SAFE	
1	0.2	0.28	BP_WaitForV3_Internal		SAFE	
1	0.3	0.38	BP_ECWait_External		SAFE	Not safe for patch to be used
1	0.4	0.48	BP_WaitForV3_External		SAFE	
1	0.5	0.58	BP_ECWait_External		SAFE	Not safe for patch to be used
1	0.6		BP_NoWait (No-Switch is closed)		SAFE	
0	0	0.08	BP_NoResponse(\$S Device)		0	
0	0.1	0.18	BP_NoResponse		1	
0	0.2	0.28	BP_NoWait		2	
0	0.3	0.38	BP_ECWait_External		SAFE	Not safe for patch to be used
0	0.4	0.48	BP_NoWait		3	
0	0.5	0.58	BP_ECWait_External		SAFE	Not safe for patch to be used
0	0.6	0.68	BP_NoWait		4	
0	0.7	0.78	RSVD		RSVD	
0	0.8	0.88	RSVD		RSVD	
0	0.9	1.0	BP_NoWait		5	

— LOGIC

2 I2C Ports or 3 I2C Port in TP565988	
	RN7403, R7470
2 I2C Ports	No ASM
3 I2C Ports	ASM



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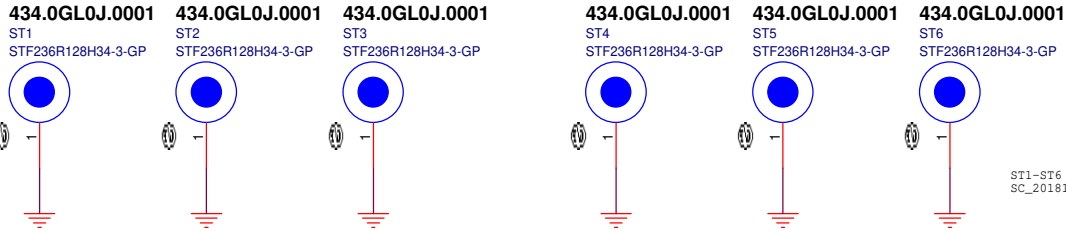
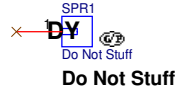
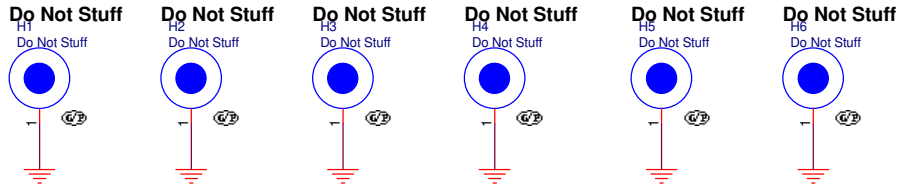
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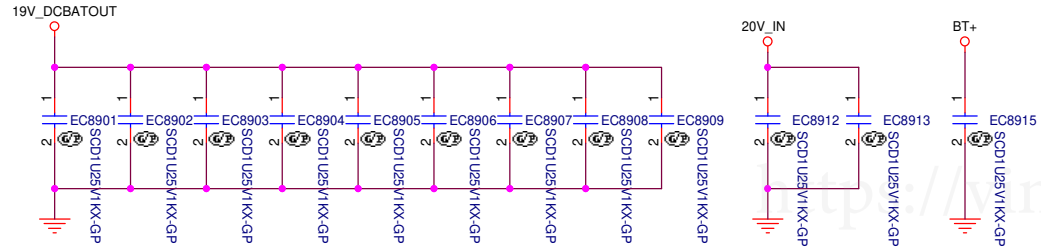
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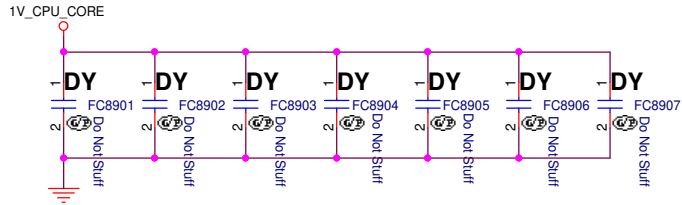
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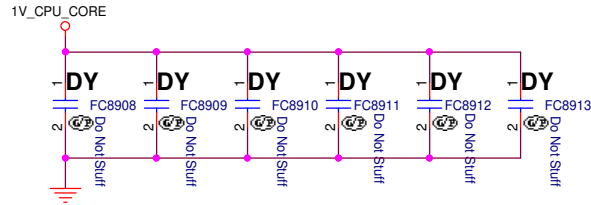
ST1-ST6 34.4YP25.001 DY-> 434.0GL0J.0001
SC_20181009



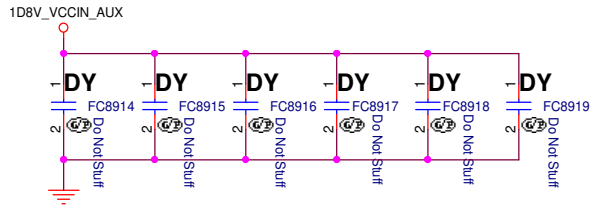
PLACE on TOP SIDE <5mm FROM SOC



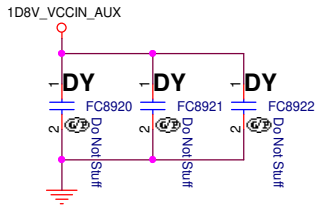
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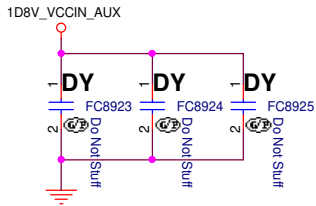
PLACE on TOP SIDE <5mm FROM SOC



PLACE on BOTTOM SIDE <5mm FROM SOC



PLACE on BOTTOM SIDE <5mm FROM SOC



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Taipei Hsien 221, Taiwan, R.O.C.

Title

UNUSED PARTS (RF/EMI CAP)

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
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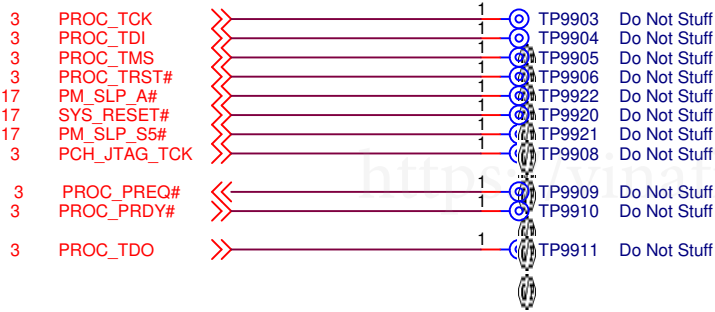
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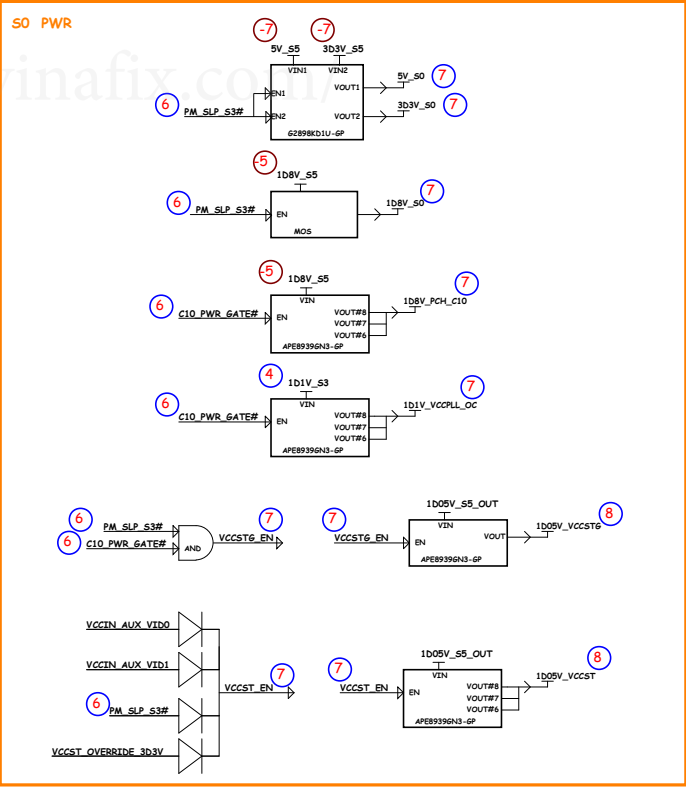
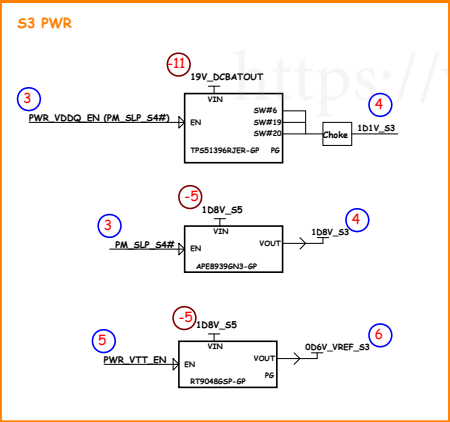
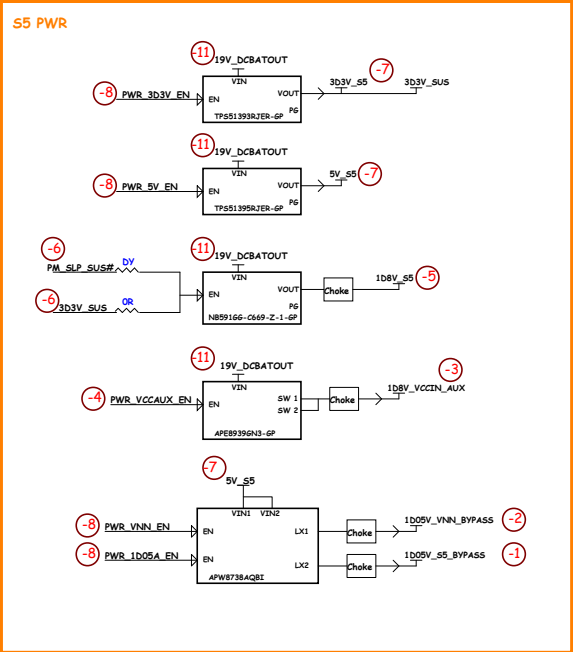
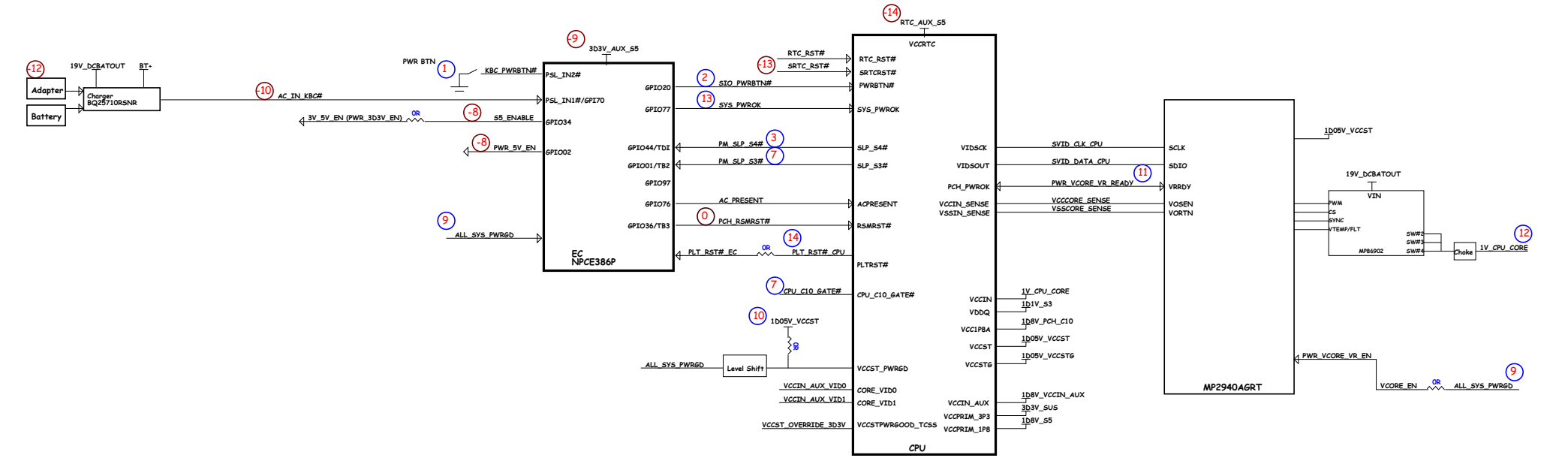
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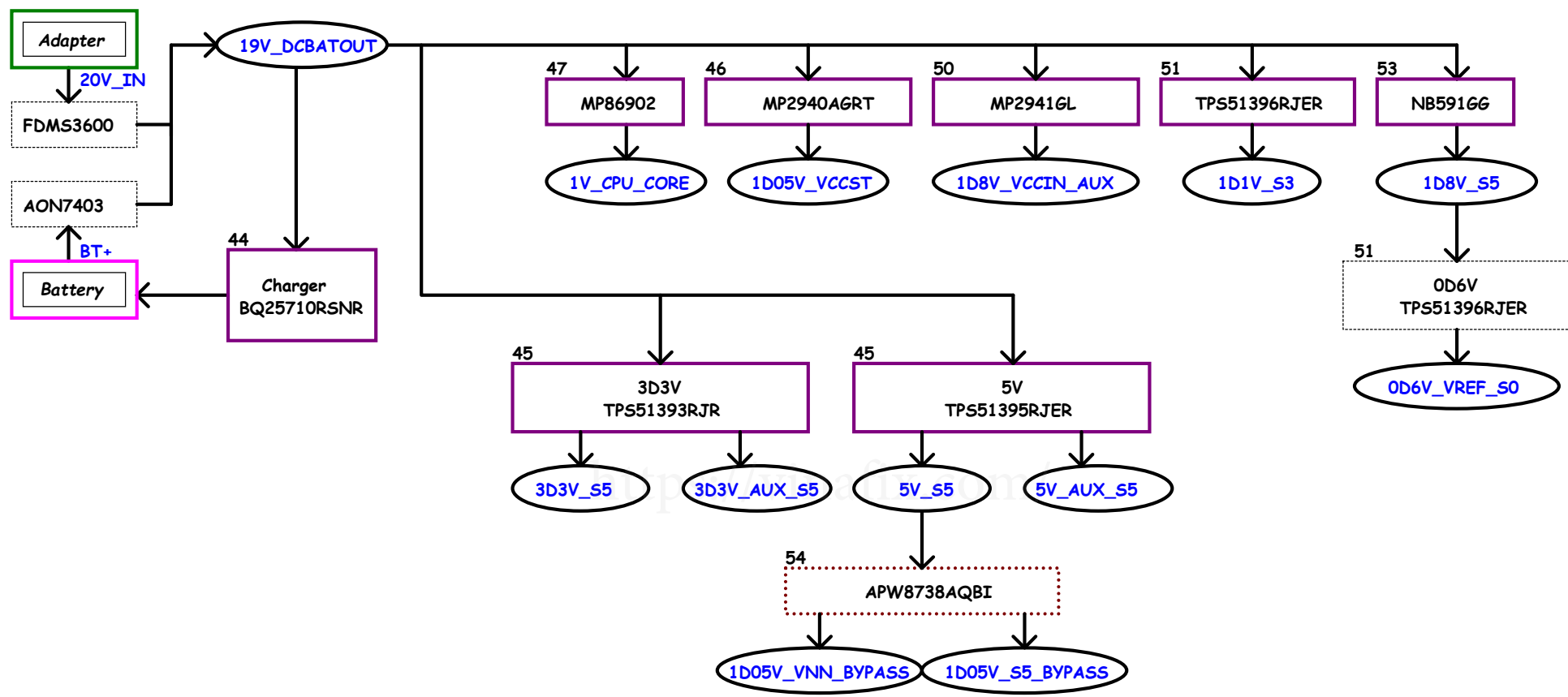
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
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LS40 ICL SEQUENCE & BLOCK DIAGRAM

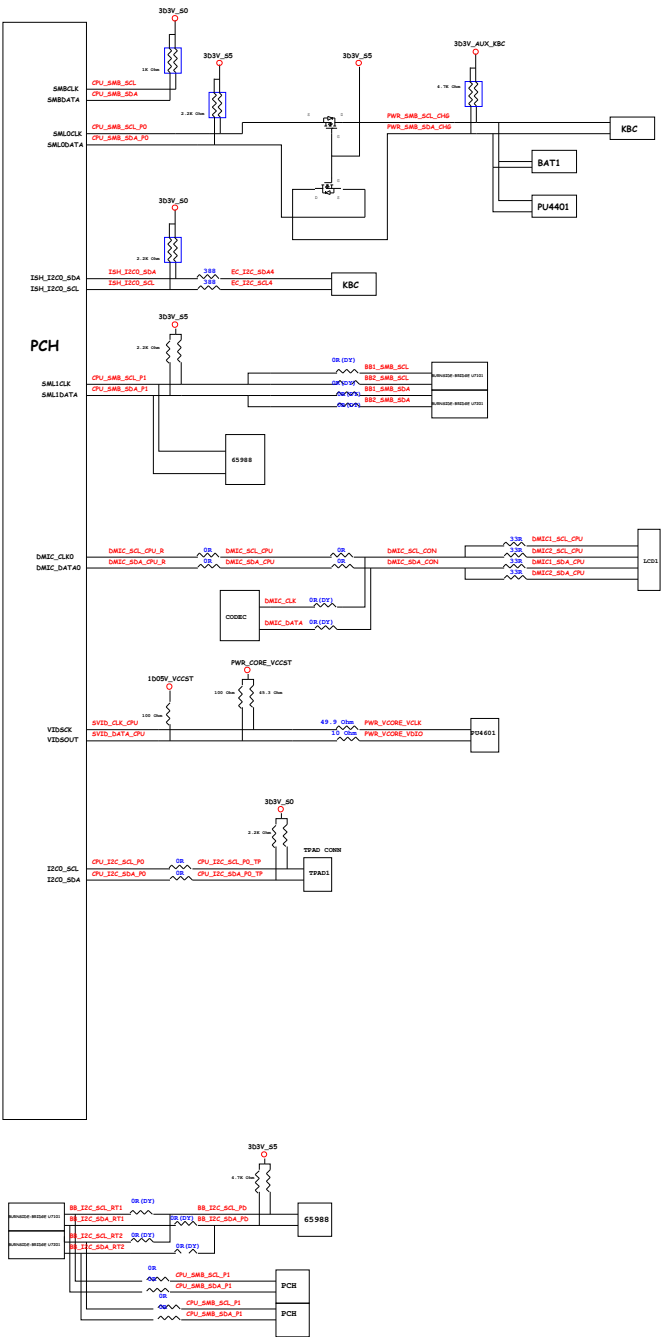


LS40 ICL Power Block Diagram

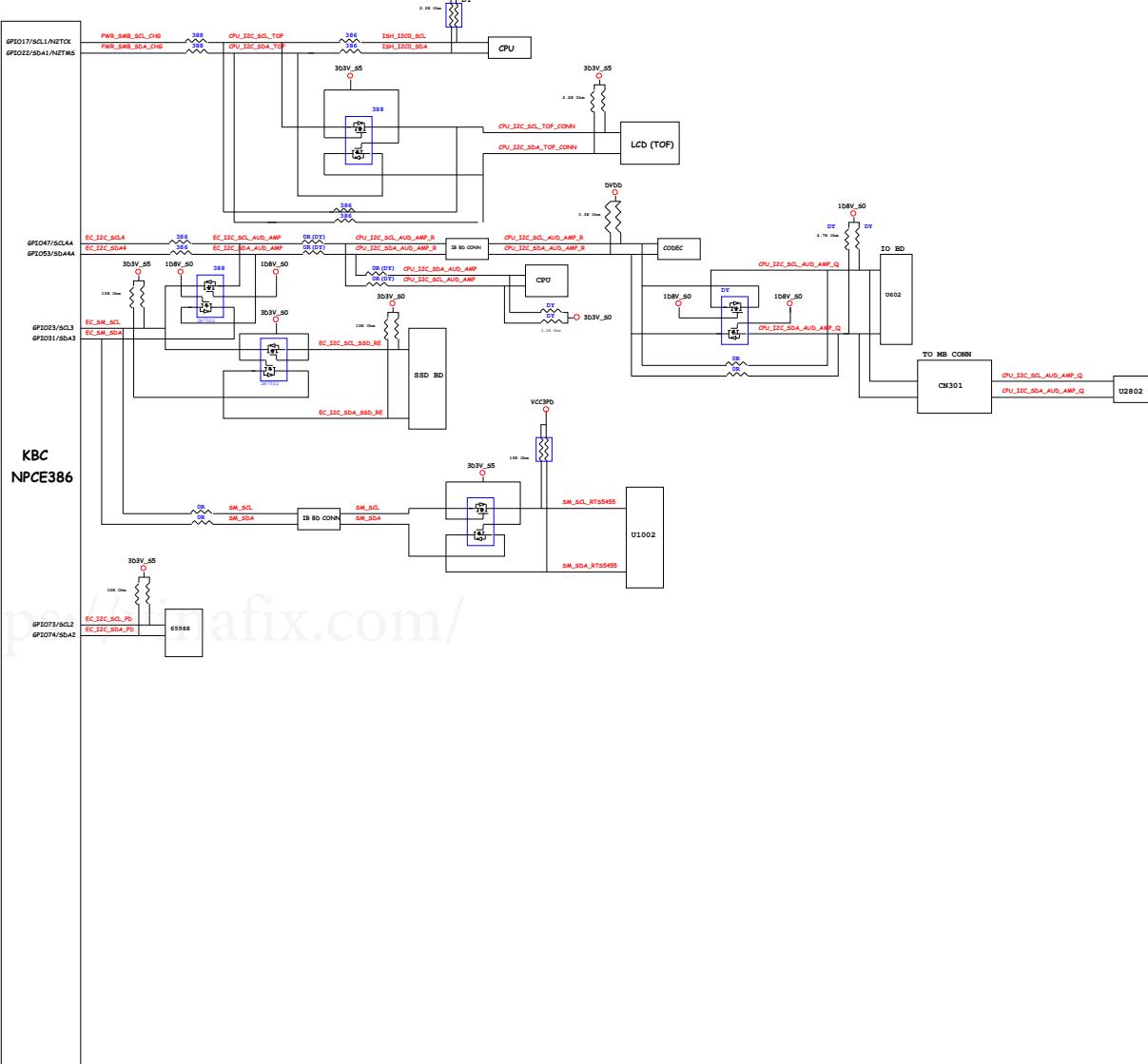


LS40 ICL SMBUS/I2C BLOCK DIAGRAM

PCH SMBus Block Diagram



KBC SMBus Block Diagram



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